MF1S50YYX_V1

MIFARE Classic EV1 1K - Mainstream contactless smart card IC for fast and easy solution development

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Product data sheet
COMPANY PUBLIC

1 General description

NXP Semiconductors has developed the MIFARE Classic EV1 contactless IC MF1S50yyX/V1 to be used in a contactless smart card according to ISO/IEC 14443 Type A.

The MIFARE Classic EV1 with 1K memory MF1S50yyX/V1 IC is used in applications like public transport ticketing and can also be used for various other applications.

1.1 Anticollision

An intelligent anticollision function allows to operate more than one card in the field simultaneously. The anticollision algorithm selects each card individually and ensures that the execution of a transaction with a selected card is performed correctly without interference from another card in the field.

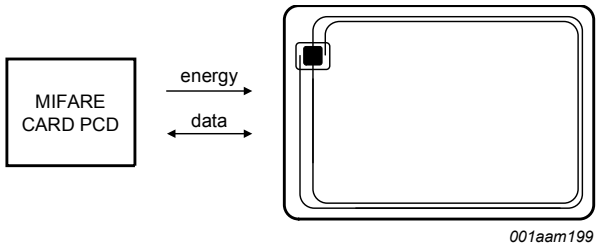


Figure 1. Contactless MIFARE product-based system

1.2 Simple integration and user convenience

The MF1S50yyX/V1 is designed for simple integration and user convenience which allows complete ticketing transactions to be handled in less than 100 ms.

1.3 Security and privacy

- Manufacturer programmed 7-byte UID or 4-byte NUID identifier for each device
- Random ID support
- Mutual three pass authentication (ISO/IEC DIS 9798-2)
- Individual set of two keys per sector to support multi-application with key hierarchy

1.4 Delivery options

- 7-byte UID, 4-byte NUID
- Bumped die on sawn wafer

- MOA4 and MOA8 contactless module

2 Features and benefits

- Contactless transmission of data and energy supply
- Operating distance up to 100 mm depending on antenna geometry and reader configuration
- Operating frequency of 13.56 MHz
- Data transfer of 106 kbit/s
- Data integrity of 16-bit CRC, parity, bit coding, bit counting
- Anticollision
- Typical ticketing transaction time of < 100 ms (including backup management)
- 7 Byte UID or 4 Byte NUID
- Random ID support (7 Byte UID version)
- NXP Originality Check support

2.1 EEPROM

- 1 kB, organized in 16 sectors of 4 blocks (one block consists of 16 byte)
- User definable access conditions for each memory block
- Data retention time of 10 years
- Write endurance 200000 cycles

3 Applications

- Public transportation
- Electronic toll collection
- School and campus cards
- Internet cafés
- Access management
- Car parking
- Employee cards
- Loyalty

4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_i	input capacitance		[1]	14.9	16.9	19.0	pF
f_i	input frequency			-	13.56	-	MHz
EEPROM characteristics							
t_{ret}	retention time	T_{amb} = 22 °C		10	-	-	year
$N_{endu(W)}$	write endurance	T_{amb} = 22 °C		100000	200000	-	cycle

[1] T_{amb}=22°C, f=13,56Mhz, V_{LaLb} = 1,5 V RMS

5 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
MF1S5001XDUD/V1	FFC Bump	8 inch wafer, 120 µm thickness, on film frame carrier, electronic fail die marking according to SECS-II format), Au bumps, 7-byte UID	-
MF1S5001XDUD2/V1	FFC Bump	12 inch wafer, 120 µm thickness, on film frame carrier, electronic fail die marking according to SECS-II format), Au bumps, 7-byte UID	-
MF1S5001XDUF/V1	FFC Bump	8 inch wafer, 75 µm thickness, on film frame carrier, electronic fail die marking according to SECS-II format), Au bumps, 7-byte UID	-
MF1S5000XDA4/V1	MOA4	plastic leadless module carrier package; 35 mm wide tape, 7-byte UID	SOT500-2
MF1S5000XDA8/V1	MOA8	plastic leadless module carrier package; 35 mm wide tape, 7-byte UID	SOT500-4
MF1S5031XDUD/V1	FFC Bump	8 inch wafer, 120 µm thickness, on film frame carrier, electronic fail die marking according to SECS-II format), Au bumps, 4-byte non-unique ID	-
MF1S5031XDUD2/V1	FFC Bump	12 inch wafer, 120 µm thickness, on film frame carrier, electronic fail die marking according to SECS-II format), Au bumps, 4-byte non-unique ID	-
MF1S5031XDUF/V1	FFC Bump	8 inch wafer, 75 µm thickness, on film frame carrier, electronic fail die marking according to SECS-II format), Au bumps, 4-byte non-unique ID	-
MF1S5030XDA4/V1	MOA4	plastic leadless module carrier package; 35 mm wide tape, 4-byte non-unique ID	SOT500-2
MF1S5030XDA8/V1	MOA8	plastic leadless module carrier package; 35 mm wide tape, 4-byte non-unique ID	SOT500-4

6 Block diagram

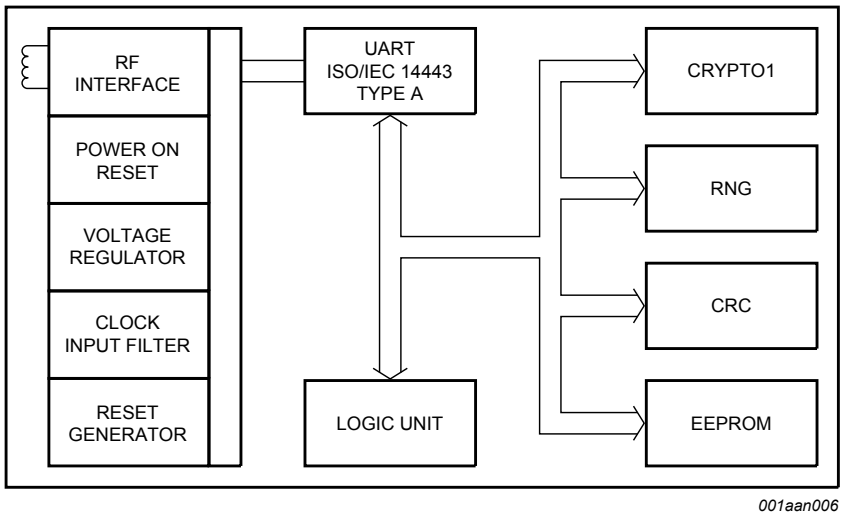


Figure 2. Block diagram of MF1S50yyX/V1

7 Pinning information

7.1 Pinning

The pinning for the MF1S50yyX/V1DAx is shown as an example in Figure 3 for the MOA4 contactless module. For the contactless module MOA8, the pinning is analogous and not explicitly shown.

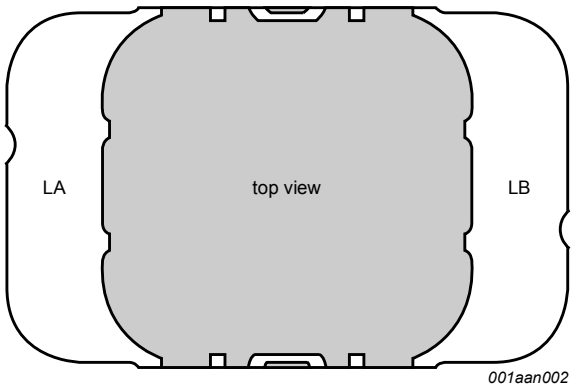


Figure 3. Pin configuration for SOT500-2 (MOA4)

Table 3. Pin allocation table

Pin	Symbol	
LA	LA	Antenna coil connection LA
LB	LB	Antenna coil connection LB

8 Functional description

8.1 Block description

The MF1S50yyX/V1 chip consists of a 1 kB EEPROM, RF interface and Digital Control Unit. Energy and data are transferred via an antenna consisting of a coil with a small number of turns which is directly connected to the MF1S50yyX/V1. No further external components are necessary. Refer to the document Ref. 1 for details on antenna design.

- RF interface:
  - Modulator/demodulator
  - Rectifier
  - Clock regenerator
  - Power-On Reset (POR)
  - Voltage regulator
- Anticollision: Multiple cards in the field may be selected and managed in sequence
- Authentication: Preceding any memory operation the authentication procedure ensures that access to a block is only possible via the two keys specified for each block

- Control and Arithmetic Logic Unit: Values are stored in a special redundant format and can be incremented and decremented
- EEPROM interface
- Crypto unit: The CRYPTO1 stream cipher of the MF1S50yyX/V1 is used for authentication and encryption of data exchange.
- EEPROM: 1 kB is organized in 16 sectors of 4 blocks. One block contains 16 bytes. The last block of each sector is called "trailer", which contains two secret keys and programmable access conditions for each block in this sector.

8.2 Communication principle

The commands are initiated by the reader and controlled by the Digital Control Unit of the MF1S50yyX/V1. The command response is depending on the state of the IC and for memory operations also on the access conditions valid for the corresponding sector.

8.2.1 Request standard / all

After Power-On Reset (POR) the card answers to a request REQA or wakeup WUPA command with the answer to request code (see Section 9.4, ATQA according to ISO/IEC 14443A).

8.2.2 Anticollision loop

In the anticollision loop the identifier of a card is read. If there are several cards in the operating field of the reader, they can be distinguished by their identifier and one can be selected (select card) for further transactions. The unselected cards return to the idle state and wait for a new request command. If the 7-byte UID is used for anticollision and selection, two cascade levels need to be processes as defined in ISO/IEC 14443-3.

Remark: For the 4-byte non-unique ID product versions, the identifier retrieved from the card is not defined to be unique. For further information regarding handling of non-unique identifiers see Ref. 6.

8.2.3 Select card

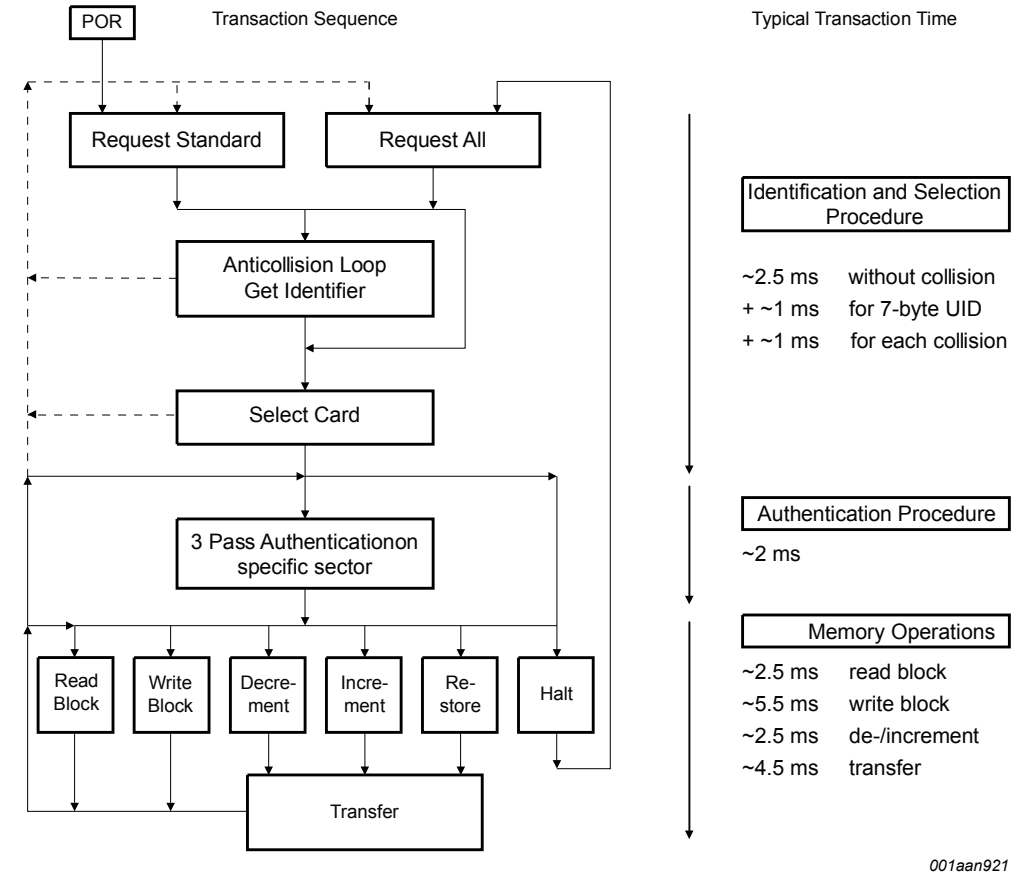
With the select card command the reader selects one individual card for authentication and memory related operations. The card returns the Select AcKnowledge (SAK) code

which determines the type of the selected card, see Section 9.4. For further details refer to the document Ref. 2.

8.2.4 Three pass authentication

After selection of a card the reader specifies the memory location of the following memory access and uses the corresponding key for the three pass authentication procedure. After a successful authentication all commands and responses are encrypted.

Remark: The HLTA command needs to be sent encrypted to the PICC after a successful authentication in order to be accepted.



1. the command flow diagram does not include the Personalize UID Usage and the SET_MOD_TYPE command, for details on those commands please see Section 10.1.1 and Section 11

Figure 4. MIFARE Classic command flow diagram

8.2.5 Memory operations

After authentication any of the following operations may be performed:

- Read block
- Write block
- Decrement: Decrements the contents of a block and stores the result in the internal Transfer Buffer
- Increment: Increments the contents of a block and stores the result in the internal Transfer Buffer
- Restore: Moves the contents of a block into the internal Transfer Buffer
- Transfer: Writes the contents of the internal Transfer Buffer to a value block

8.3 Data integrity

Following mechanisms are implemented in the contactless communication link between reader and card to ensure very reliable data transmission:

- 16 bits CRC per block
- Parity bits for each byte

- Bit count checking
- Bit coding to distinguish between "1", "0" and "no information"
- Channel monitoring (protocol sequence and bit stream analysis)

8.4 Three pass authentication sequence

1. The reader specifies the sector to be accessed and chooses key A or B.
2. The card reads the secret key and the access conditions from the sector trailer. Then the card sends a number as the challenge to the reader (pass one).
3. The reader calculates the response using the secret key and additional input. The response, together with a random challenge from the reader, is then transmitted to the card (pass two).
4. The card verifies the response of the reader by comparing it with its own challenge and then it calculates the response to the challenge and transmits it (pass three).
5. The reader verifies the response of the card by comparing it to its own challenge.

After transmission of the first random challenge the communication between card and reader is encrypted.

8.5 RF interface

The RF-interface is according to the standard for contactless smart cards ISO/IEC 14443A.

For operation, the carrier field from the reader always needs to be present (with short pauses when transmitting), as it is used for the power supply of the card.

For both directions of data communication there is only one start bit at the beginning of each frame. Each byte is transmitted with a parity bit (odd parity) at the end. The LSB of the byte with the lowest address of the selected block is transmitted first. The maximum frame length is 163 bits (16 data bytes + 2 CRC bytes = 16 × 9 + 2 × 9 + 1 start bit).

8.6 Memory organization

The 1024 × 8 bit EEPROM memory is organized in 16 sectors of 4 blocks. One block contains 16 bytes.

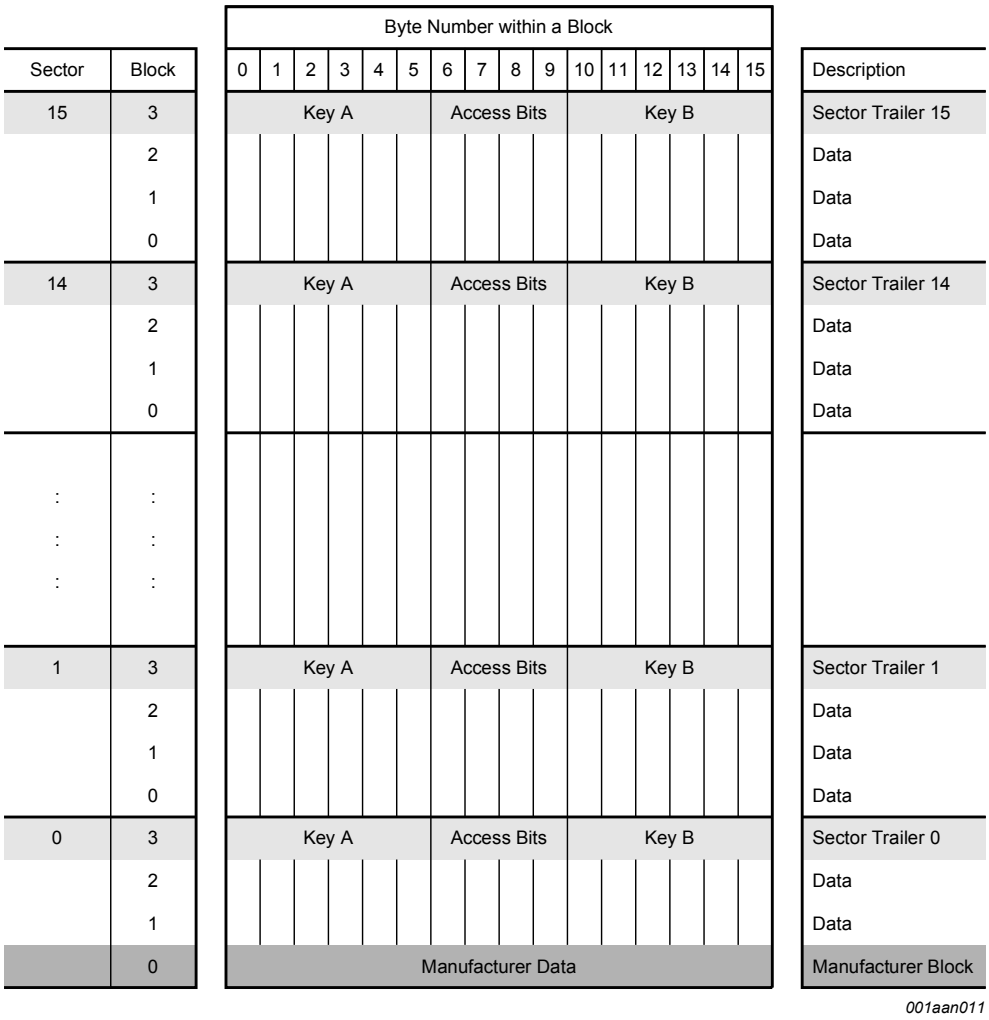


Figure 5. Memory organization

8.6.1 Manufacturer block

This is the first data block (block 0) of the first sector (sector 0). It contains the IC manufacturer data. This block is programmed and write protected in the production test. The manufacturer block is shown in Figure 6 and Figure 7 for the 4-byte NUID and 7-byte UID version respectively.

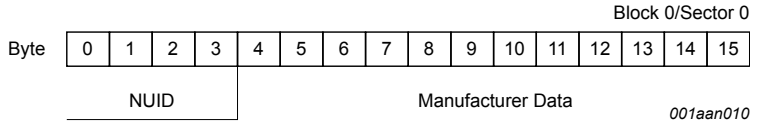


Figure 6. Manufacturer block for MF1S503yX with 4-byte NUID

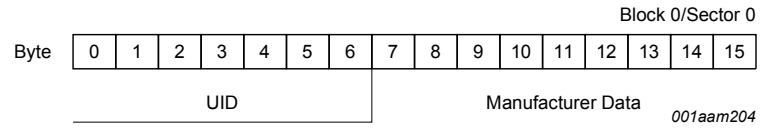


Figure 7. Manufacturer block for MF1S500yX with 7-byte UID

8.6.2 Data blocks

All sectors contain 3 blocks of 16 bytes for storing data (Sector 0 contains only two data blocks and the read-only manufacturer block).

The data blocks can be configured by the access bits as

- read/write blocks
- value blocks

Value blocks can be used for e.g. electronic purse applications, where additional commands like increment and decrement for direct control of the stored value are provided

A successful authentication has to be performed to allow any memory operation.

Remark: The default content of the data blocks at delivery is not defined.

8.6.2.1 Value blocks

Value blocks allow performing electronic purse functions (valid commands are: read, write, increment, decrement, restore, transfer). Value blocks have a fixed data format which permits error detection and correction and a backup management.

A value block can only be generated through a write operation in value block format:

- Value: Signifies a signed 4-byte value. The lowest significant byte of a value is stored in the lowest address byte. Negative values are stored in standard 2´s complement format. For reasons of data integrity and security, a value is stored three times, twice non-inverted and once inverted.
- Adr: Signifies a 1-byte address, which can be used to save the storage address of a block, when implementing a powerful backup management. The address byte is stored four times, twice inverted and non-inverted. During increment, decrement, restore and transfer operations the address remains unchanged. It can only be altered via a write command.

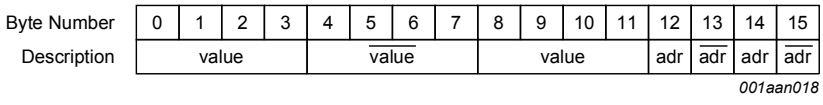


Figure 8. Value blocks

An example of a valid value block format for the decimal value 1234567d and the block address 17d is shown in Table 4. First, the decimal value has to be converted to the hexadecimal representation of 0012D687h. The LSByte of the hexadecimal value is stored in Byte 0, the MSByte in Byte 3. The bit inverted hexadecimal representation of the value is FFED2978h where the LSByte is stored in Byte 4 and the MSByte in Byte 7.

The hexadecimal value of the address in the example is 11h, the bit inverted hexadecimal value is EEh.

Table 4. Value block format example

Byte Number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Description	value				value				value				adr	$\overline{adr}$	adr	$\overline{adr}$
Values [hex]	87	D6	12	00	78	29	ED	FF	87	D6	12	00	11	EE	11	EE

8.6.3 Sector trailer

The sector trailer is the last block (block 3) in one sector. Each sector has a sector trailer containing the

- secret keys A (mandatory) and B (optional), which return logical "0"s when read and
- the access conditions for the blocks of that sector, which are stored in bytes 6...9. The access bits also specify the type (data or value) of the data blocks.

If key B is not needed, the last 6 bytes of the sector trailer can be used as data bytes. The access bits for the sector trailer have to be configured accordingly, see Section 8.7.2.

Byte 9 of the sector trailer is available for user data. For this byte the same access rights as for byte 6, 7 and 8 apply.

When the sector trailer is read, the key bytes are blanked out by returning logical zeros. If key B is configured to be readable, the data stored in bytes 10 to 15 is returned, see Section 8.7.2.

All keys are set to FFFF FFFF FFFFh at chip delivery and the bytes 6, 7 and 8 are set to FF0780h.

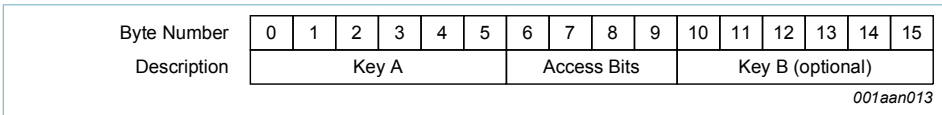


Figure 9. Sector trailer

8.7 Memory access

Before any memory operation can be done, the card has to be selected and authenticated as described in Section 8.2. The possible memory operations for an addressed block depend on the key used during authentication and the access conditions stored in the associated sector trailer.

Table 5. Memory operations

Operation	Description	Valid for Block Type
Read	reads one memory block	read/write, value and sector trailer
Write	writes one memory block	read/write, value and sector trailer
Increment	increments the contents of a block and stores the result in the internal Transfer Buffer	value
Decrement	decrements the contents of a block and stores the result in the internal Transfer Buffer	value

Operation	Description	Valid for Block Type
Transfer	writes the contents of the internal Transfer Buffer to a block	value and read/write
Restore	reads the contents of a block into the internal Transfer Buffer	value

8.7.1 Access conditions

The access conditions for every data block and sector trailer are defined by 3 bits, which are stored non-inverted and inverted in the sector trailer of the specified sector.

The access bits control the rights of memory access using the secret keys A and B. The access conditions may be altered, provided one knows the relevant key and the current access condition allows this operation.

Remark: With each memory access the internal logic verifies the format of the access conditions. If it detects a format violation the whole sector is irreversibly blocked.

Remark: In the following description the access bits are mentioned in the non-inverted mode only.

The internal logic of the MF1S50yyX/V1 ensures that the commands are executed only after a successful authentication.

Table 6. Access conditions

Access Bits	Valid Commands		Block	Description
$C1_3$, $C2_3$, $C3_3$	read, write	→	3	sector trailer
$C1_2$, $C2_2$, $C3_2$	read, write, increment, decrement, transfer, restore	→	2	data block
$C1_1$, $C2_1$, $C3_1$	read, write, increment, decrement, transfer, restore	→	1	data block
$C1_0$,$C2_0$, $C3_0$	read, write, increment, decrement, transfer, restore	→	0	data block

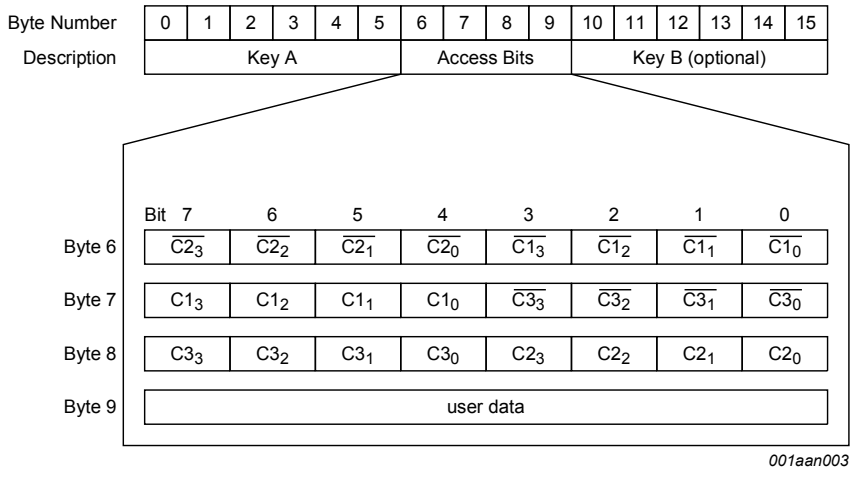


Figure 10. Access conditions

8.7.2 Access conditions for the sector trailer

Depending on the access bits for the sector trailer (block 3) the read/write access to the keys and the access bits is specified as ‘never’, ‘key A’, ‘key B’ or key A|B’ (key A or key B).

On chip delivery the access conditions for the sector trailers and key A are predefined as transport configuration. Since key B may be read in the transport configuration, new cards must be authenticated with key A. Since the access bits themselves can also be blocked, special care has to be taken during the personalization of cards.

Table 7. Access conditions for the sector trailer

Access bits			Access condition for						Remark
			KEYA		Access bits		KEYB		
C1	C2	C3	read	write	read	write	read	write	
0	0	0	never	key A	key A	never	key A	key A	Key B may be read[1]
0	1	0	never	never	key A	never	key A	never	Key B may be read[1]
1	0	0	never	key B	key A|B	never	never	key B	
1	1	0	never	never	key A|B	never	never	never	
0	0	1	never	key A	key A	key A	key A	key A	Key B may be read, transport configuration[1]
0	1	1	never	key B	key A|B	key B	never	key B	
1	0	1	never	never	key A|B	key B	never	never	
1	1	1	never	never	key A|B	never	never	never	

[1] For this access condition key B is readable and may be used for data

8.7.3 Access conditions for data blocks

Depending on the access bits for data blocks (blocks 0...2) the read/write access is specified as ‘never’, ‘key A’, ‘key B’ or ‘key A|B’ (key A or key B). The setting of the relevant access bits defines the application and the corresponding applicable commands.

- Read/write block: the operations read and write are allowed.
- Value block: Allows the additional value operations increment, decrement, transfer and restore. With access condition ‘001’ only read and decrement are possible which reflects a non-rechargeable card. For access condition ‘110’ recharging is possible by using key B.
- Manufacturer block: the read-only condition is not affected by the access bits setting!
- Key management: in transport configuration key A must be used for authentication

Table 8. Access conditions for data blocks

Access bits			Access condition for				Application
C1	C2	C3	read	write	increment	decrement, transfer, restore	
0	0	0	key A|B	key A|B	key A|B	key A|B	transport configuration[1]

Access bits			Access condition for				Application
0	1	0	key A|B	never	never	never	read/write block[1]
1	0	0	key A|B	key B	never	never	read/write block[1]
1	1	0	key A|B	key B	key B	key A|B	value block[1]
0	0	1	key A|B	never	never	key A|B	value block[1]
0	1	1	key B	key B	never	never	read/write block[1]
1	0	1	key B	never	never	never	read/write block[1]
1	1	1	never	never	never	never	read/write block

[1] If key B may be read in the corresponding Sector Trailer it cannot serve for authentication (see grey marked lines in Table 7). As a consequences, if the reader authenticates any block of a sector which uses such access conditions for the Sector Trailer and using key B, the card will refuse any subsequent memory access after authentication.

9 Command overview

Note: *In this document the term „MIFARE Classic card“ refers to a MIFARE Classic IC-based contactless card.*

The MIFARE Classic card activation follows the ISO/IEC 14443 Type A. After the MIFARE Classic card has been selected, it can either be deactivated using the ISO/IEC 14443 Halt command, or the MIFARE Classic commands can be performed. For more details about the card activation refer to Ref. 4.

9.1 MIFARE Classic command overview

All MIFARE Classic commands typically use the MIFARE Classic using Crypto1 and require an authentication.

All available commands for the MIFARE Classic EV1 with 1K memory are shown in Table 9.

Table 9. Command overview

Command	ISO/IEC 14443	Command code (hexadecimal)
Request	REQA	26h (7 bit)
Wake-up	WUPA	52h (7 bit)
Anticollision CL1	Anticollision CL1	93h 20h
Select CL1	Select CL1	93h 70h
Anticollision CL2	Anticollision CL2	95h 20h
Select CL2	Select CL2	95h 70h
Halt	Halt	50h 00h
Authentication with Key A	-	60h
Authentication with Key B	-	61h
Personalize UID Usage	-	40h
SET_MOD_TYPE	-	43h
MIFARE Read	-	30h

Command	ISO/IEC 14443	Command code (hexadecimal)
MIFARE Write	-	A0h
MIFARE Decrement	-	C0h
MIFARE Increment	-	C1h
MIFARE Restore	-	C2h
MIFARE Transfer	-	B0h

All commands use the coding and framing as described in Ref. 3 and Ref. 4 if not otherwise specified.

9.2 Timings

The timing shown in this document are not to scale and values are rounded to 1 µs.

All given times refer to the data frames including start of communication and end of communication. A PCD data frame contains the start of communication (1 "start bit") and the end of communication (one logic 0 + 1 bit length of unmodulated carrier). A PICC data frame contains the start of communication (1 "start bit") and the end of communication (1 bit length of no subcarrier).

The minimum command response time is specified according to Ref. 4 as an integer n which specifies the PCD to PICC frame delay time. The frame delay time from PICC to PCD is at least 87 µs. The maximum command response time is specified as a time-out value. Depending on the command, the T_{ACK} value specified for command responses defines the PCD to PICC frame delay time. It does it for either the 4-bit ACK value specified in Section 9.3 or for a data frame.

All command timings are according to ISO/IEC 14443-3 frame specification as shown for the Frame Delay Time in Figure 11. For more details refer to Ref. 3 and Ref. 4.

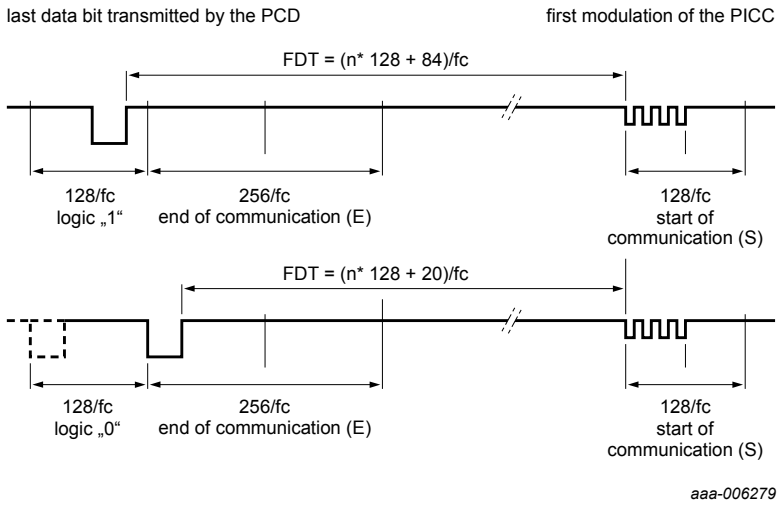


Figure 11. Frame Delay Time (from PCD to PICC) and T_{ACK} and T_{NAK}

Remark: Due to the coding of commands, the measured timings usually excludes (a part of) the end of communication. Consider this factor when comparing the specified with the measured times.

9.3 MIFARE Classic ACK and NAK

The MIFARE Classic uses a 4 bit ACK / NAK as shown in Table 10.

Table 10. MIFARE ACK and NAK

Code (4-bit)	Transfer Buffer Validity	Description
Ah		Acknowledge (ACK)
0h	valid	invalid operation
1h	valid	parity or CRC error
4h	invalid	invalid operation
5h	invalid	parity or CRC error

9.4 ATQA and SAK responses

For details on the type identification procedure please refer to Ref. 2.

The MF1S50yyX/V1 answers to a REQA or WUPA command with the ATQA value shown in Table 11 and to a Select CL1 command (CL2 for the 7-byte UID variant) with the SAK value shown in Table 12.

Table 11. ATQA response of the MF1S50yyX/V1

		Bit Number														
Sales Type	Hex Value	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
MF1S500yX	00 44h	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
MF1S503yX	00 04h	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
MF1S700yX	$00\ 42_h$	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0
MF1S703yX	$00\ 02_h$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Table 12. SAK response of the MF1S50yyX/V1

		Bit Number							
Sales Type	Hex Value	8	7	6	5	4	3	2	1
MF1S50yyX/V1	08h	0	0	0	0	1	0	0	0

Remark: The ATQA coding in bits 7 and 8 indicate the UID size according to ISO/IEC 14443 independent from the settings of the UID usage.

Remark: The bit numbering in the ISO/IEC 14443 starts with LSBit = bit 1, but not LSBit = bit 0. So one byte counts bit 1 to 8 instead of bit 0 to 7.

10 UID Options and Handling

The MF1S50yyX/V1 product family offers two delivery options for the UID which is stored in block 0 of sector 0.

- 7-byte UID
- 4-byte NUID (Non-Unique ID)

This section describes the MIFARE Classic MF1S50yyX/V1 operation when using one of the 2 UID options with respect to card selection, authentication and personalization. See also Ref. 6 for details on how to handle UIDs and NUIDs with MIFARE Classic products.

10.1 7-byte UID Operation

All MF1S50**0**yXDyy products are featuring a 7-byte UID. This 7-byte UID is stored in block 0 of sector 0 as shown in Figure 7. The behaviour during anti-collision, selection and authentication can be configured during personalization for this UID variant.

10.1.1 Personalization Options

The 7-byte UID variants of the MF1S50yyX/V1 can be operated with four different functionalities, denoted as UIDFn (UID Functionality n).

1. UIDF0: anti-collision and selection with the double size UID according to ISO/IEC 14443-3
2. UIDF1: anti-collision and selection with the double size UID according to ISO/IEC 14443-3 and optional usage of a selection process shortcut
3. UIDF2: anti-collision and selection with a single size random ID according to ISO/IEC 14443-3
4. UIDF3: anti-collision and selection with a single size NUID according to ISO/IEC 14443-3 where the NUID is calculated out of the 7-byte UID

The anti-collision and selection procedure and the implications on the authentication process are detailed in Section 10.1.2 and Section 10.1.3.

The default configuration at delivery is option 1 which enables the ISO/IEC 14443-3 compliant anti-collision and selection. This configuration can be changed using the ‘Personalize UID Usage’ command. The execution of this command requires an authentication to sector 0. Once this command has been issued and accepted by the PICC, the configuration is automatically locked. A subsequently issued ‘Personalize UID Usage’ command is not executed and a NAK is replied by the PICC.

Remark: As the configuration is changeable at delivery, it is strongly recommended to send this command at personalization of the card to prevent unwanted changes in the field. This should also be done if the default configuration is used.

Remark: The configuration becomes effective only after PICC unselect or PICC field reset.

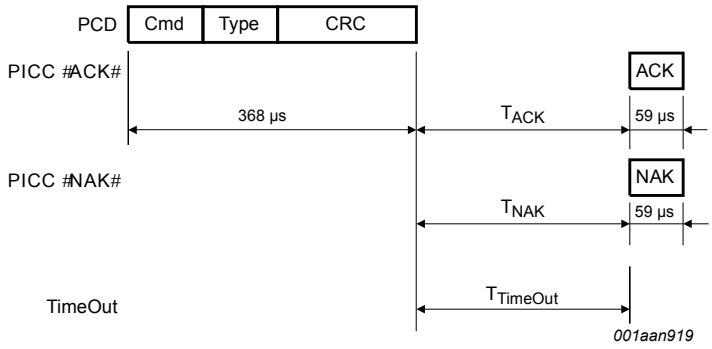


Figure 12. Personalize UID Usage

Table 13. Personalize UID Usage command

Name	Code	Description	Length
Cmd	40h	Set anti-collision, selection and authentication behaviour	1 byte
Type	-	Encoded type of UID usage: UIDF0: 00h UIDF1: 40h UIDF2: 20h UIDF3: 60h	1 byte
CRC	-	CRC according to Ref. 4	2 bytes
ACK, NAK	see Table 10	see Section 9.3	4-bit

Table 14. Personalize UID Usage timing

	T_{ACK} min	T_{ACK} max	T_{NAK} min	T_{NAK} max	$T_{TimeOut}$
Personalize UID Usage	n=9	$T_{TimeOut}$	n=9	$T_{TimeOut}$	10 ms

10.1.2 Anti-collision and Selection

Depending on the chosen personalization option there are certain possibilities to perform anti-collision and selection. To bring the MIFARE Classic contactless IC into the ACTIVE state according to ISO/IEC 14443-3, the following sequences are available.

Sequence 1: ISO/IEC 14443-3 compliant anti-collision and selection using the cascade level 1 followed by the cascade level 2 SEL command

Sequence 2: using cascade level 1 anti-collision and selection procedure followed by a Read command from block 0

Sequence 3: ISO/IEC 14443-3 compliant anti-collision and selection using the cascade level 1 SEL command

Remark: The Read from Block 0 in Sequence 2 does not require a prior authentication to Sector 0 and is transmitted in plain data. For all other sequences, the readout from Block 0 in Sector 0 is encrypted and requires an authentication to that sector.

Remark: The settings done with Personalize UID Usage do not change the ATQA coding.

Table 15. Available activation sequences for 7-byte UID options

UID Functionality	Available Activation Sequences
UIDF0	Sequence 1
UIDF1	Sequence 1, Sequence 2
UIDF2	Sequence 3
UIDF3	Sequence 3

10.1.3 Authentication

During the authentication process, 4-byte of the UID are passed on to the MIFARE Classic Authenticate command of the contactless reader IC. Depending on the activation sequence, those 4-byte are chosen differently. In general, the input parameter to the MIFARE Classic Authenticate command is the set of 4 bytes retrieved during the last cascade level from the ISO/IEC 14443-3 Type A anticollision.

Table 16. Input parameter to MIFARE Classic Authenticate

UID Functionality	Input to MIFARE Classic Authenticate Command
Sequence 1	CL2 bytes (UID3...UID6)
Sequence 2	CL1 bytes (CT, UID0...UID2)
Sequence 3	4-byte NUID/RID (UID0...UID3)

10.2 4-byte UID Operation

All MF1S50**3**yXDyy products are featuring a 4-byte NUID. This 4-byte NUID is stored in block 0 of sector 0 as shown in Figure 6.

10.2.1 Anti-collision and Selection

The anti-collision and selection process for the product variants featuring 4-byte NUIDs is done according to ISO/IEC 14443-3 Type A using cascade level 1 only.

10.2.2 Authentication

The input parameter to the MIFARE Classic Authenticate command is the full 4-byte UID retrieved during the anti-collision procedure. This is the same as for the activation Sequence 3 in the 7-byte UID variant.

11 Load Modulation Strength Option

The MIFARE Classic EV1 with 1K memory features the possibility to set the load modulation strength to high or normal. The default level is set to a high modulation strength and it is recommended for optimal performance to maintain this level and only switch to the low load modulation strength if the contactless system requires it.

Remark: The configuration becomes effective only after a PICC unselect or a PICC field reset. The configuration can be changed multiple times by asserting the command.

Remark: The MIFARE Classic EV1 with 1K memory needs to be authenticated to sector 0 with Key A to perform the SET_MOD_TYPE command. The Access Bits for sector 0 are irrelevant.

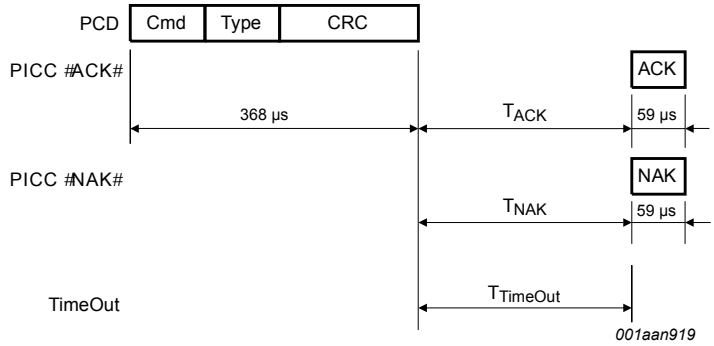


Figure 13. SET_MOD_TYPE

Table 17. SET_MOD_TYPE command

Name	Code	Description	Length
Cmd	43h	Set load modulation strength	1 byte
Type	-	Encoded load modulation strength: strong modulation: 01h (default) normal modulation: 00h	1 byte
CRC	-	CRC according to Ref. 4	2 bytes
ACK, NAK	see Table 10	see Section 9.3	4-bit

Table 18. SET_MOD_TYPE timing

	T_{ACK} min	T_{ACK} max	T_{NAK} min	T_{NAK} max	$T_{TimeOut}$
SET_MOD_TYPE	n=9	$T_{TimeOut}$	n=9	$T_{TimeOut}$	5 ms

The configured load modulation is shown in the manufacturer data of block 0 in sector 0. The exact location is shown below in Figure 14 and Table 19.

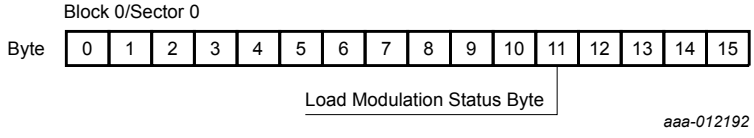


Figure 14. Byte Location of Load Modulation Status in Block 0 / Sector 0

Table 19. Load Modulation Status Indication

		Bit Number							
Load Modulation Type	**Hex Value**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
strong load modulation	20h (default)	0	0	1	0	0	0	0	0
normal load modulation	00h	0	0	0	0	0	0	0	0

12 MIFARE Classic commands

12.1 MIFARE Classic Authentication

The MIFARE Classic authentication is a 3-pass mutual authentication which needs two pairs of command-response. These two parts, MIFARE Classic authentication part 1 and part 2 are shown in Figure 15, Figure 16 and Table 20.

Table 21 shows the required timing.

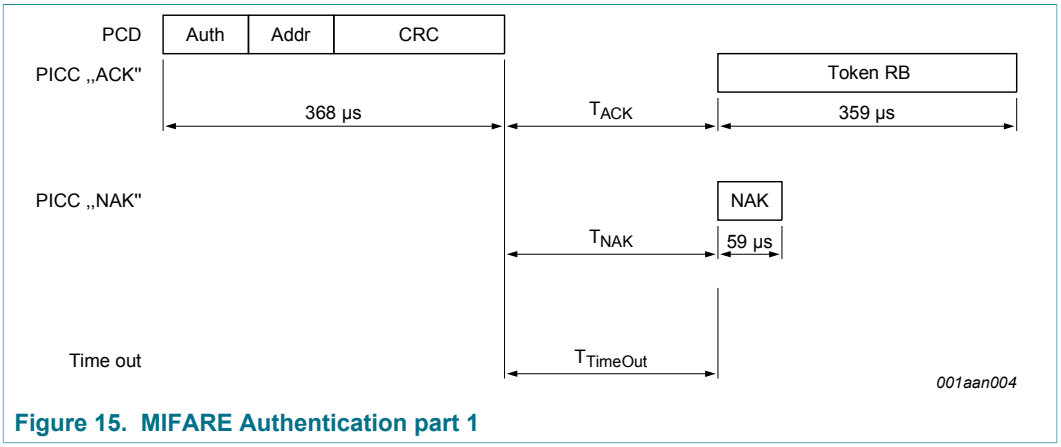


Figure 15. MIFARE Authentication part 1

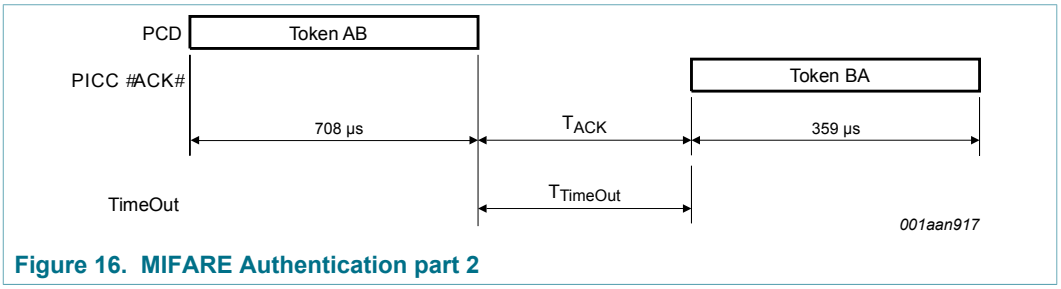


Figure 16. MIFARE Authentication part 2

Table 20. MIFARE Classic authentication command

Name	Code	Description	Length
Auth (with Key A)	60h	Authentication with Key A	1 byte
Auth (with Key B)	61h	Authentication with Key B	1 byte
Addr	-	MIFARE Block address (00h to FFh)	1 byte
CRC	-	CRC according to Ref. 4	2 bytes
Token RB	-	Challenge 1 (Random Number)	4 bytes
Token AB	-	Challenge 2 (encrypted data)	8 bytes
Token BA	-	Challenge 2 (encrypted data)	4 bytes
NAK	see Table 10	see Section 9.3	4-bit

Table 21. MIFARE Classic authentication timing

	T_{ACK} min	T_{ACK} max	T_{NAK} min	T_{NAK} max	$T_{TimeOut}$
Authentication part 1	n=9	$T_{TimeOut}$	n=9	n=9	1 ms
Authentication part 2	n=9	$T_{TimeOut}$			1 ms

Remark: The minimum required time between MIFARE Classic Authentication part 1 and part 2 is the minimum required FDT according to Ref. 4. There is no maximum time specified.

Remark: The MIFARE Classic authentication and encryption requires an NFC reader IC for MIFARE products (e.g. the CL RC632). For more details about the authentication command refer to the corresponding data sheet (e.g. Ref. 5). The 4-byte input parameter for the MIFARE Classic Authentication is detailed in Section 10.1.3 and Section 10.2.2.

12.2 MIFARE Read

The MIFARE Read requires a block address, and returns the 16 bytes of one MIFARE Classic block. The command structure is shown in Figure 17 and Table 22.

Table 23 shows the required timing.

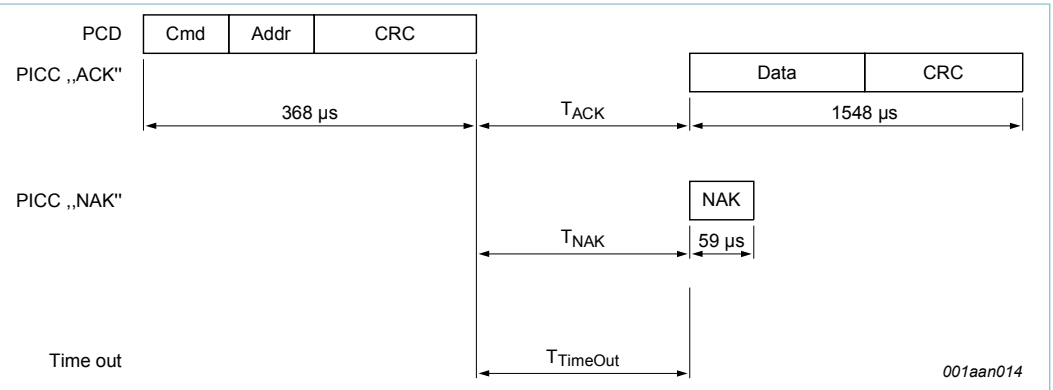


Figure 17. MIFARE Read

Table 22. MIFARE Read command

Name	Code	Description	Length
Cmd	30h	Read one block	1 byte
Addr	-	MIFARE Block address (00h to FFh)	1 byte
CRC	-	CRC according to Ref. 4	2 bytes
Data	-	Data content of the addressed block	16 bytes
NAK	see Table 10	see Section 9.3	4-bit

Table 23. MIFARE Read timing

	T_{ACK} min	T_{ACK} max	T_{NAK} min	T_{NAK} max	$T_{TimeOut}$
Read	n=9	$T_{TimeOut}$	n=9	$T_{TimeOut}$	5 ms

12.3 MIFARE Write

The MIFARE Write requires a block address, and writes 16 bytes of data into the addressed MIFARE Classic EV1 with 1K memory block. It needs two pairs of command-response. These two parts, MIFARE Write part 1 and part 2 are shown in Figure 18 and Figure 19 and Table 24.

Table 25 shows the required timing.

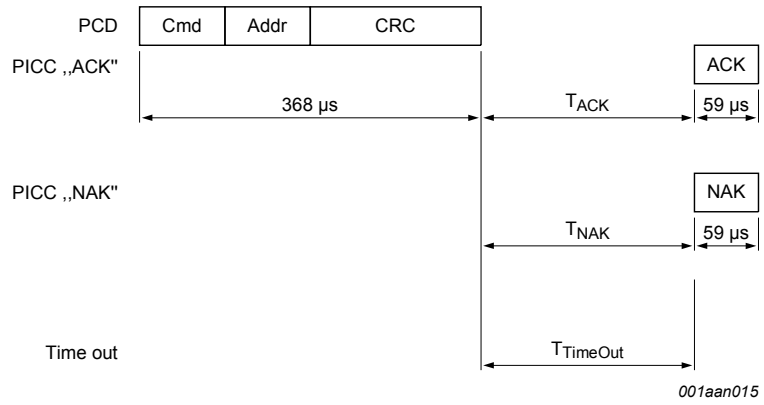


Figure 18. MIFARE Write part 1

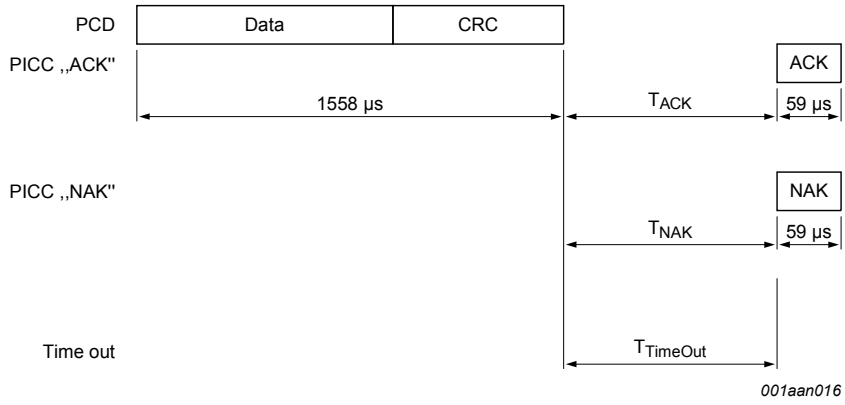


Figure 19. MIFARE Write part 2

Table 24. MIFARE Write command

Name	Code	Description	Length
Cmd	A0h	Write one block	1 byte
Addr	-	MIFARE Block or Page address (00h to FFh)	1 byte
CRC	-	CRC according to Ref. 4	2 bytes
Data	-	Data	16 bytes
NAK	see Table 10	see Section 9.3	4-bit

Table 25. MIFARE Write timing

	T_{ACK} min	T_{ACK} max	T_{NAK} min	T_{NAK} max	$T_{TimeOut}$
Write part 1	n=9	$T_{TimeOut}$	n=9	$T_{TimeOut}$	5 ms
Write part 2	n=9	$T_{TimeOut}$	n=9	$T_{TimeOut}$	10 ms

Remark: The minimum required time between MIFARE Write part 1 and part 2 is the minimum required FDT according to Ref. 4. There is no maximum time specified.

12.4 MIFARE Increment, Decrement and Restore

The MIFARE Increment requires a source block address and an operand. It adds the operand to the value of the addressed block, and stores the result in the Transfer Buffer.

The MIFARE Decrement requires a source block address and an operand. It subtracts the operand from the value of the addressed block, and stores the result in the Transfer Buffer.

The MIFARE Restore requires a source block address. It copies the value of the addressed block into the Transfer Buffer. The 4 byte Operand in the second part of the command is not used and may contain arbitrary values.

All three commands are responding with a NAK to the first command part if the addressed block is not formatted to be a valid value block, see Section 8.6.2.1.

The two parts of each command are shown in Figure 20 and Figure 21 and Table 26.

Table 27 shows the required timing.

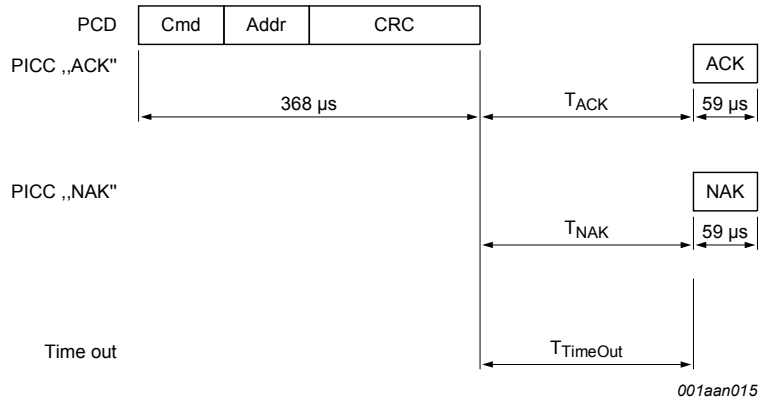
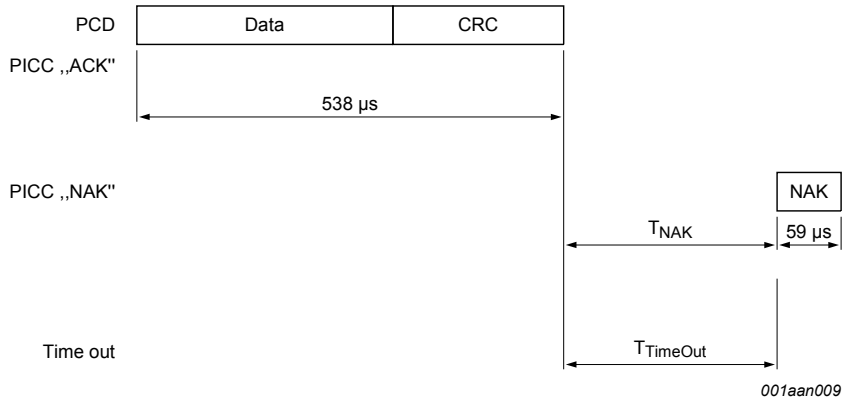


Figure 20. MIFARE Increment, Decrement, Restore part 1



1. Increment, Decrement and Restore part 2 does not acknowledge

Figure 21. MIFARE Increment, Decrement, Restore part 2

Table 26. MIFARE Increment, Decrement and Restore command

Name	Code	Description	Length
Cmd	C1h	Increment	1 byte
Cmd	C0h	Decrement	1 byte
Cmd	C2h	Restore	1 byte
Addr	-	MIFARE source block address (00h to FFh)	1 byte
CRC	-	CRC according to Ref. 4	2 bytes
Data	-	Operand (4 byte signed integer)	4 bytes
NAK	see Table 10	see Section 9.3	4-bit

Table 27. MIFARE Increment, Decrement and Restore timing

	T_{ACK} min	T_{ACK} max	T_{NAK} min	T_{NAK} max	$T_{TimeOut}$
Increment, Decrement, and Restore part 1	n=9	$T_{TimeOut}$	n=9	$T_{TimeOut}$	5 ms
Increment, Decrement, and Restore part 2	n=9	$T_{TimeOut}$	n=9	$T_{TimeOut}$	5 ms

Remark: The minimum required time between MIFARE Increment, Decrement, and Restore part 1 and part 2 is the minimum required FDT according to Ref. 4. There is no maximum time specified.

Remark: The MIFARE Increment, Decrement, and Restore commands require a MIFARE Transfer to store the value into a destination block.

Remark: The MIFARE Increment, Decrement, and Restore command part 2 does not provide an acknowledgement, so the regular time out has to be used instead.

12.5 MIFARE Transfer

The MIFARE Transfer requires a destination block address, and writes the value stored in the Transfer Buffer into one MIFARE Classic block. The command structure is shown in Figure 22 and Table 28.

Table 29 shows the required timing.

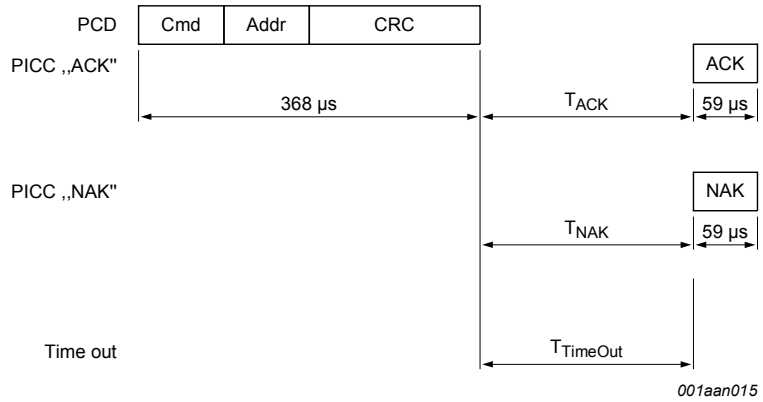


Figure 22. MIFARE Transfer

Table 28. MIFARE Transfer command

Name	Code	Description	Length
Cmd	B0h	Write the value from the Transfer Buffer into destination block	1 byte
Addr	-	MIFARE destination block address (00h to FFh)	1 byte
CRC	-	CRC according to Ref. 4	2 bytes
NAK	see Table 10	see Section 9.3	4-bit

Table 29. MIFARE Transfer timing

	T_{ACK} min	T_{ACK} max	T_{NAK} min	T_{NAK} max	$T_{TimeOut}$
Transfer	n=9	$T_{TimeOut}$	n=9	$T_{TimeOut}$	10 ms

13 Limiting values

Stresses above one or more of the limiting values may cause permanent damage to the device. Exposure to limiting values for extended periods may affect device reliability.

Table 30. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter		Min	Max	Unit
I_I	input current		-	30	mA
P_{tot}/pack	total power dissipation per package		-	120	mW

Symbol	Parameter		Min	Max	Unit
T_{stg}	storage temperature		-55	125	°C
T_{amb}	ambient temperature		-25	70	°C
V_{ESD}	electrostatic discharge voltage on LA/LB	[1]	2	-	kV

[1] ANSI/ESDA/JEDEC JS-001; Human body model: C = 100 pF, R = 1.5 kΩ

CAUTION

This device has limited built-in ElectroStatic Discharge (ESD) protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the gates.

14 Characteristics

Table 31. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_i	input capacitance		[1]	14.9	16.9	19.0	pF
f_i	input frequency			-	13.56	-	MHz
EEPROM characteristics							
t_{ret}	retention time	T_{amb} = 22 °C		10	-	-	year
$N_{endu(W)}$	write endurance	T_{amb} = 22 °C		100000	200000	-	cycle

[1] T_{amb}=22°C, f=13,56Mhz, V_{LaLb} = 1,5 V RMS

15 Wafer specification

For more details on the wafer delivery forms see Ref. 9.

Table 32. Wafer specifications MF1S50yyXDUy

Wafer	
diameter	200 mm typical (8 inches) 300 mm typical (12 inches)
maximum diameter after foil expansion	210 mm (8 inches) not applicable (12 inches)
die seperation process	laser dicing (8 inches) blade dicing (12 inches)
thickness MF1S50yyXDUD	120 µm ± 15 µm
MF1S50yyXDUF	75 µm ± 10 µm
flatness	not applicable
Potential Good Dies per Wafer (PGDW)	64727 (8 inches) 147540 (12 inches)
Wafer backside	
material	Si

treatment	ground and stress relieve
roughness	R_a max = 0.5 µm
	R_t max = 5 µm
Chip dimensions	
step size[1]	x = 658 µm (8 inches) x = 660 µm (12 inches)
	y = 713 µm (8 inches) y = 715 µm (12 inches)
gap between chips[1]	typical = 19 µm
	minimum = 5 µm not applicable (12 inches)
Passivation	
type	sandwich structure
material	PSG / nitride
thickness	500 nm / 600 nm
Au bump (substrate connected to VSS)	
material	> 99.9 % pure Au
hardness	35 to 80 HV 0.005
shear strength	> 70 MPa
height	18 µm
height uniformity	within a die = ±2 µm
	within a wafer = ±3 µm
	wafer to wafer = ±4 µm
flatness	minimum = ±1.5 µm
size	LA, LB, VSS, TEST[2] = 66 µm × 66 µm
size variation	±5 µm
under bump metallization	sputtered TiW

[1] The step size and the gap between chips may vary due to changing foil expansion
[2] Pads VSS and TESTIO are disconnected when wafer is sawn.

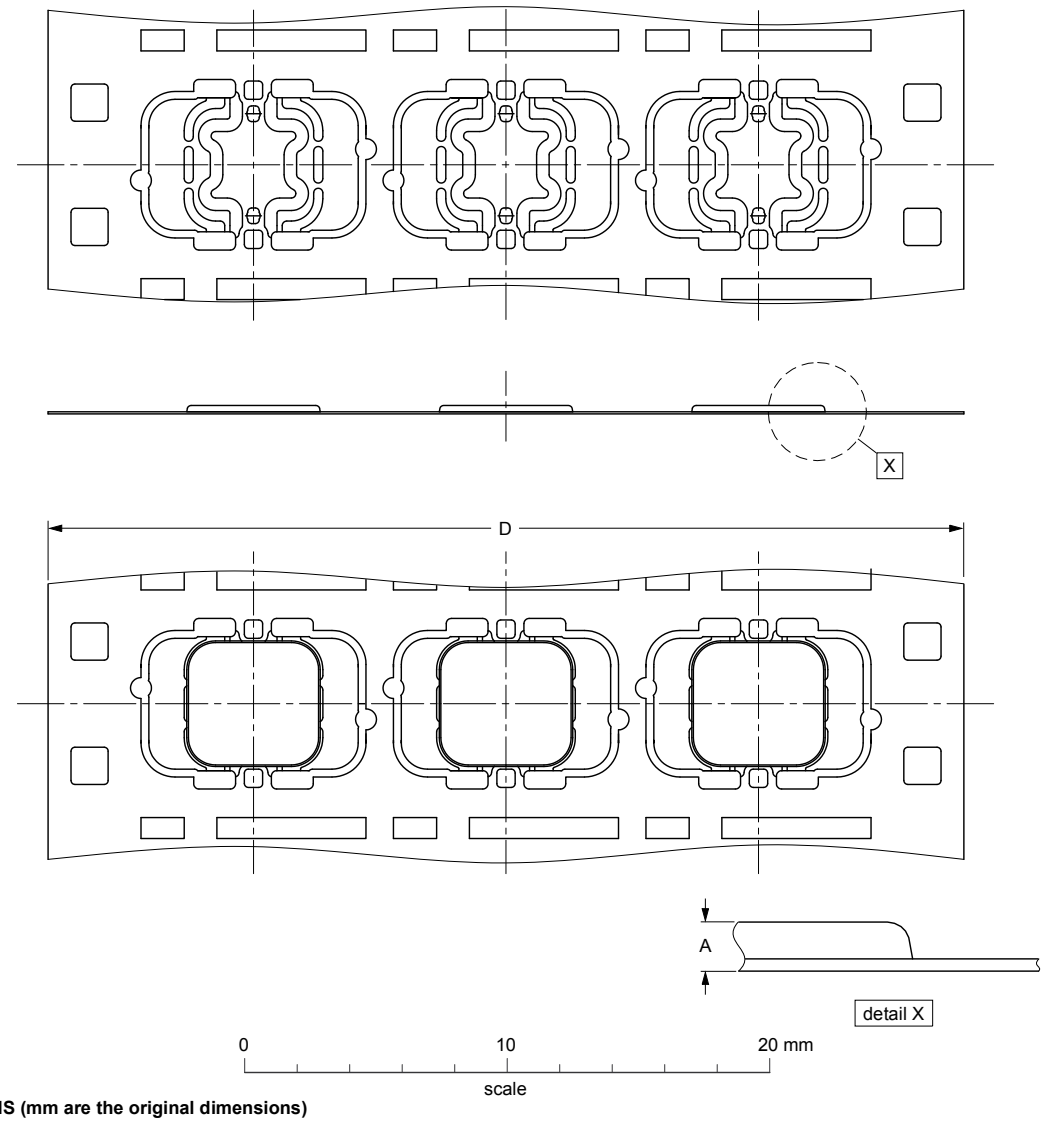
15.1 Fail die identification

Electronic wafer mapping covers the electrical test results and additionally the results of mechanical/visual inspection. No ink dots are applied.

15.2 Package outline

For more details on the contactless modules MOA4 and MOA8 please refer to Ref. 7 and Ref. 8.

PLLMC: plastic leadless module carrier package; 35 mm wide tape **SOT500-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	D	
mm	0.33	35.05 34.95	For unspecified dimensions see PLLMC-drawing given in the subpackage code.

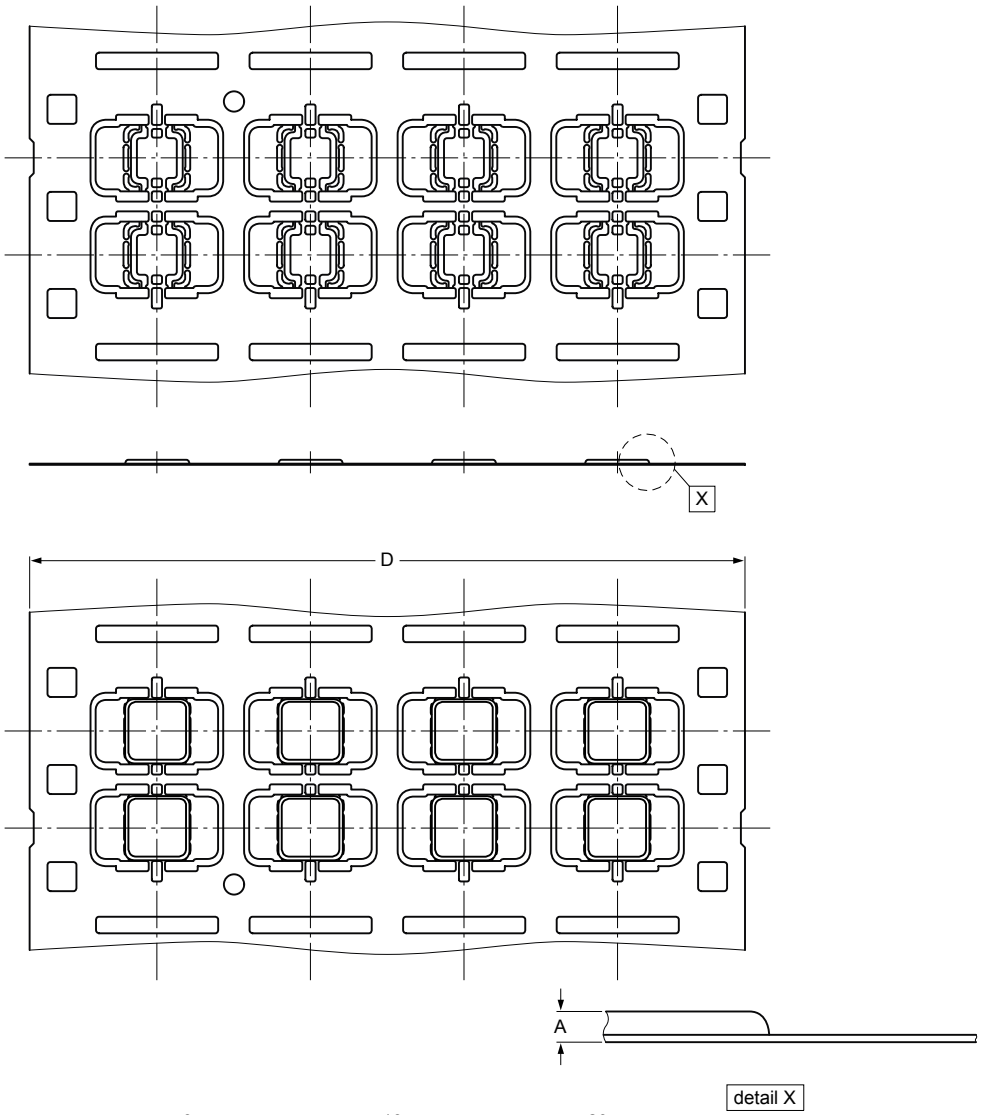
Note

1. Total package thickness, exclusive punching burr.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT500-2	- - -	- - -	- - -			~~03-09-17~~ 06-05-22

Figure 23. Package outline SOT500-2

PLLMC: plastic leadless module carrier package; 35 mm wide tape **SOT500-4**



Dimensions

Unit		$A^{(1)}$	D
mm	max	0.26	35.05
	nom		35.00
	min		34.95

For unspecified dimensions see PLLMC-drawing given in the subpackage code.

Note
1. Total package thickness, exclusive punching burr.

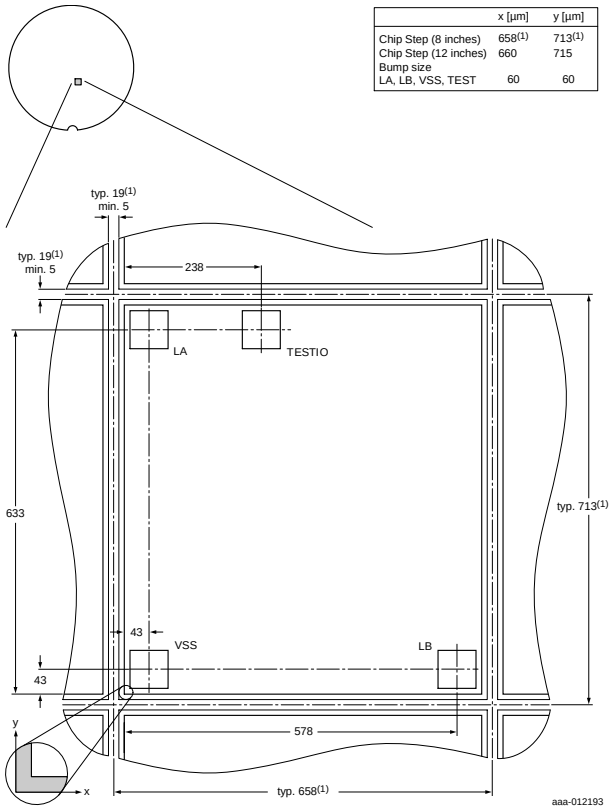
sot500-4_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT500-4	- - -	- - -	- - -			11-02-18

Figure 24. Package outline SOT500-4

16 Bare die outline

For more details on the wafer delivery forms, see Ref. 9.



1. Laser dicing: The air gap and thus the step size may vary due to varying foil expansion
2. All dimensions in µm, pad locations measured from metal ring edge (see detail)

Figure 25. Bare die outline MF1S50yyXDUz/V1

17 Abbreviations

Table 33. Abbreviations and symbols

Acronym	Description
ACK	ACKnowledge
ATQA	Answer To reQuest, Type A
CRC	Cyclic Redundancy Check
CT	Cascade Tag (value 88h) as defined in ISO/IEC 14443-3 Type A
EEPROM	Electrically Erasable Programmable Read-Only Memory
FDT	Frame Delay Time
FFC	Film Frame Carrier
IC	Integrated Circuit
LCR	L = inductance, Capacitance, Resistance (LCR meter)
LSB	Least Significant Bit

Acronym	Description
NAK	Not AcKnowledge
NUID	Non-Unique IDentifier
NV	Non-Volatile memory
PCD	Proximity Coupling Device (Contactless Reader)
PICC	Proximity Integrated Circuit Card (Contactless Card)
REQA	REQuest command, Type A
RID	Random ID
RF	Radio Frequency
RMS	Root Mean Square
RNG	Random Number Generator
SAK	Select AcKnowledge, type A
SECS-II	SEMI Equipment Communications Standard part 2
TiW	Titanium Tungsten
UID	Unique IDentifier
WUPA	Wake-Up Protocol type A

18 References

[1]

MIFARE (Card) Coil Design Guide

Application note, BU-ID Document number 0117**[1]

[2]

MIFARE Type Identification Procedure

Application note, BU-ID Document number 0184**[1]

[3]

ISO/IEC 14443-2

2001

[4]

ISO/IEC 14443-3

2001

[5]

MIFARE & I-CODE CL RC632 Multiple protocol contactless reader IC

Product data sheet

[6]

MIFARE product and handling of UIDs

1 ** ... document version number

Application note, BU-ID Document number 1907**[1]

[7]

Contactless smart card module specification MOA4

Delivery Type Description, BU-ID Document number 0823**[1]

[8]

Contactless smart card module specification MOA8

Delivery Type Description, BU-ID Document number 1636**[1]

[9]

General specification for 8" wafer on UV-tape; delivery types

Delivery Type Description, BU-ID Document number 1005**[1]

19 Revision history

Table 34. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
MF1S50yyX/V1 v.3.2	20180523	Product data sheet	-	MF1S50yyX/V1 v.3.1
Modifications:	• Editorial updates.			
MF1S50yyX/V1 v.3.1	20171121	Product data sheet	-	MF1S50yyX/V1 v.3.0
Modifications:	• 12 inch FFC delivery forms added • Format updated			
MF1S50yyX/V1 v.3.0	20140303	Product data sheet	-	-

20 Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
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