hynix

200pin Unbuffered DDR SDRAM SO-DIMMs based on 256Mb D ver. (TSOP)

This Hynix unbuffered Small Outline, Dual In-Line Memory Module (DIMM) series consists of 256Mb D ver. DDR SDRAMs in 400 mil TSOP II packages on a 200pin glass-epoxy substrate. This Hynix 256Mb D ver. based unbuffered SO-DIMM series provide a high performance 8 byte interface in 67.60mm width form factor of industry standard. It is suitable for easy interchange and addition.

FEATURES

- JEDEC Standard 200-pin small outline, dual in-line memory module (SO-DIMM)
- Two ranks 32M x 64 and One rank 32M x 64, 16M x 64 organization
- 2.6V ± 0.1V VDD and VDDQ Power supply for DDR400, 2.5V ± 0.2V for DDR333 and below
- All inputs and outputs are compatible with SSTL_2 interface
- Fully differential clock operations (CK & /CK) with 133/166/200MHz
- DLL aligns DQ and DQS transition with CK transition
- Programmable CAS Latency: DDR266(2, 2.5 clock), DDR333(2.5 clock), DDR400(3 clock)
- Programmable Burst Length 2 / 4 / 8 with both sequential and interleave mode
- Edge-aligned DQS with data outs and Center-aligned DQS with data inputs
- Auto refresh and self refresh supported
- 8192 refresh cycles / 64ms
- Serial Presence Detect (SPD) with EEPROM
- Built with 256Mb DDR SDRAMs in 400 mil TSOP II packages
- Lead-free product listed for each configuration (RoHS compliant)

ADDRESS TABLE

	Organization	Ranks	SDRAMs	# of DRAMs	# of row/bank/column Address	Refresh Method
256MB	32M x 64	2	16Mb x 16	8	13(A0~A12)/2(BA0,BA1)/9(A0~A8)	8K / 64ms
256MB	32M x 64	1	32Mb x 8	8	13(A0~A12)/2(BA0,BA1)/10(A0~A9)	8K / 64ms
128MB	16M x 64	1	16Mb x 16	4	13(A0~A12)/2(BA0,BA1)/9(A0~A8)	8K / 64ms

PERFORMANCE RANGE

Part-Number Suffix		-D43[1]	-J	-K	-H	Unit
Speed Bin		DDR400B	DDR333	DDR266A	DDR266B	-
CL - tRCD- tRP		3-3-3	2.5-3-3	2-3-3	2.5-3-3	CK
Max Clock Frequency	**CL=3**	200	-	-	-	MHz
	CL=2.5	166	166	133	133	MHz
	CL=2	133	133	133	133	MHz

Note:
1. 2.6V +/- 0.1V VDD and VDDQ Power supply for DDR400 and 2.5V +/- 0.2V for DDR333 and below

This document is a general product description and is subject to change without notice. Hynix Semiconductor does not assume any responsibility for use of circuits described. No patent licenses are implied.

ORDERING INFORMATION

Part Number	Density	Organization	Ranks	# of DRAMs	Material	DIMM Dimension
HYMD216M646D[L]6-D43/J/K/H	128MB	16M x 64	1	4	Normal	67.60 x 31.75 x 3.8 [mm^3]
HYMD216M646D[L]P6-D43/J/K/H	128MB	16M x 64	1	4	Lead-free[1]	↑
HYMD232M646D[L]8-D43/J/K/H	256MB	32M x 64	1	8	Normal	↑
HYMD232M646D[L]P8-D43/J/K/H	256MB	32M x 64	1	8	Lead-free[1]	↑
HYMD232M646D[L]6-D43/J/K/H	256MB	32M x 64	2	8	Normal	↑
HYMD232M646D[L]P6-D43/J/K/H	256MB	32M x 64	2	8	Lead-free[1]	↑

Note:
1. The "Pb-free" products contain Lead less than 0.1% by weight and satisfy RoHS - please contact Hynix for product availability.

* These products are built with HY5DU564(8,16)22DT[L][P] the Hynix DDR SDRAM component.

PIN DESCRIPTION

Pin	Pin Description	Pin	Pin Description
CK0~2, /CK0~2	Differential Clock Inputs	VDD	Power Supply for Core and I/O
/CS0, /CS1	Chip Select Inputs	VSS	Ground
CKE0, CKE1	Clock Enable Inputs	VREF	Input/Output Reference
/RAS, /CAS, /WE	Commend Sets Inputs	VDDSPD	Power Supply for SPD
A0 ~ A13	Address Inputs	VDDID	VDD, VDDQ Level Detection
A10/AP	Address Input/Autoprecharge	SA0~SA2	SPD Address Inputs
BA0, BA1	Bank Address	SCL	SPD Clock Input
DQ0~DQ63	Data Inputs/Outputs	SDA	SPD Data Input/Output
CB0~CB7	Data Check bits	DU	Do not Use
DQS0~DQS8	Data Strobes	NC	No Connection
DM0~8	Data-in Masks	TEST	Reserved for test equipment use

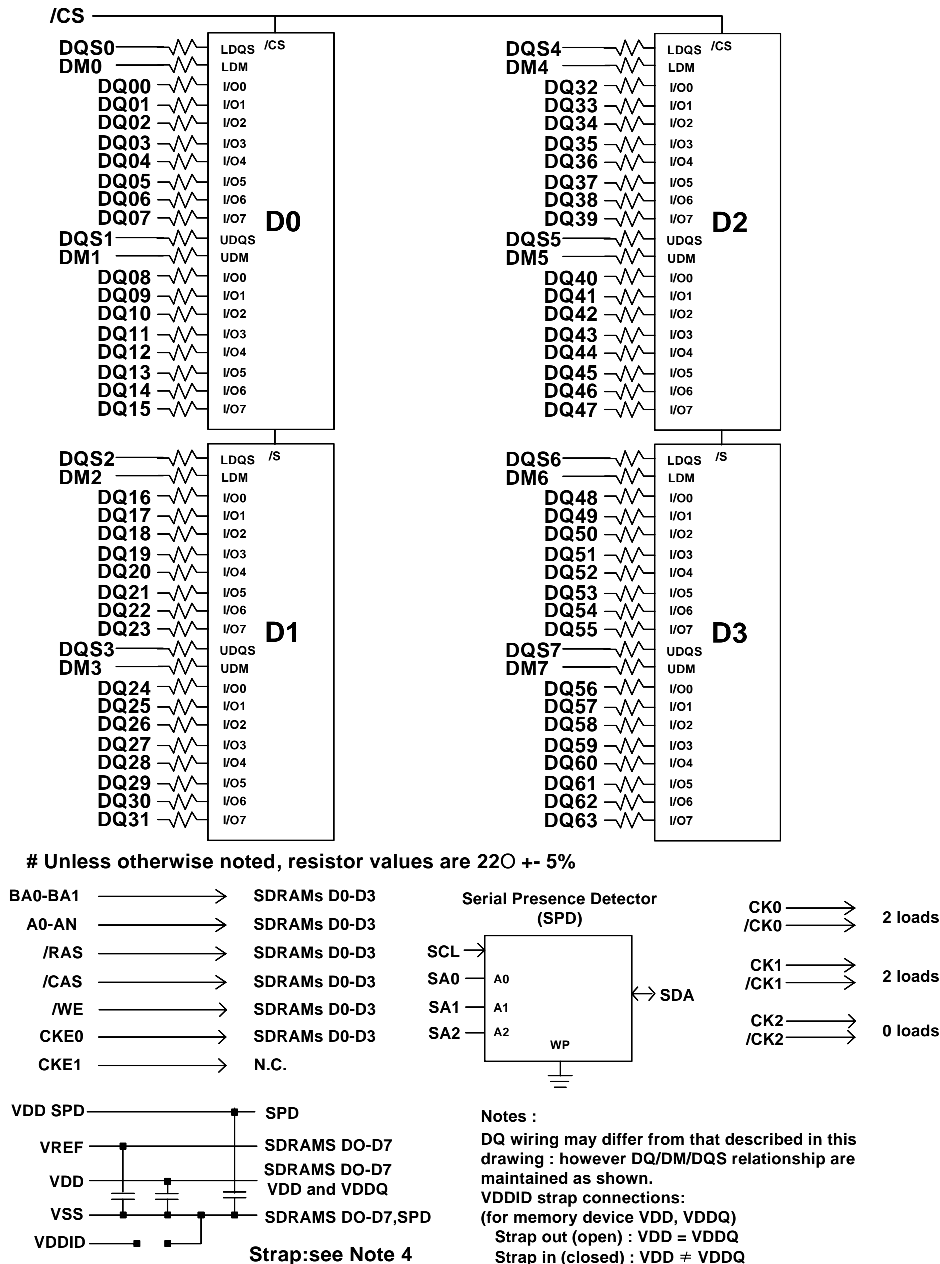
PIN ASSIGNMENT

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREF	2	VREF	51	VSS	52	VSS	101	A9	102	A8	151	DQ42	152	DQ46
3	VSS	4	VSS	53	DQ19	54	DQ23	103	VSS	104	VSS	153	DQ43	154	DQ47
5	DQ0	6	DQ4	55	DQ24	56	DQ28	105	A7	106	A6	155	VDD	156	VDD
7	DQ1	8	DQ5	57	VDD	58	VDD	107	A5	108	A4	157	VDD	158	/CK1
9	VDD	10	VDD	59	DQ25	60	DQ29	109	A3	110	A2	159	VSS	160	CK1
11	DQS0	12	DM0	61	DQS3	62	DM3	111	A1	112	A0	161	VSS	162	VSS
13	DQ2	14	DQ6	63	VSS	64	VSS	113	VDD	114	VDD	163	DQ48	164	DQ52
15	VSS	16	VSS	65	DQ26	66	DQ30	115	A10,AP	116	BA1	165	DQ49	166	DQ53
17	DQ3	18	DQ7	67	DQ27	68	DQ31	117	BA0	118	/RAS	167	VDD	168	VDD
19	DQ8	20	DQ12	69	VDD	70	VDD	119	/WE	120	/CAS	169	DQS6	170	DM6
21	VDD	22	VDD	71	CB0	72	CB4	121	/CS0	122	/CS1	171	DQ50	172	DQ54
23	DQ9	24	DQ13	73	CB1	74	CB5	123	NC,A13	124	DU	173	VSS	174	VSS
25	DQS1	26	DM1	75	VSS	76	VSS	125	VSS	126	VSS	175	DQ51	176	DQ55
27	VSS	28	VSS	77	DQS8	78	DM8	127	DQ32	128	DQ36	177	DQ56	178	DQ60
29	DQ10	30	DQ14	79	CB2	80	CB6	129	DQ33	130	DQ37	179	VDD	180	VDD
31	DQ11	32	DQ15	81	VDD	82	VDD	131	VDD	132	VDD	181	DQ57	182	DQ61
33	VDD	34	VDD	83	CB3	84	CB7	133	DQS4	134	DM4	183	DQS7	184	DM7
35	CK0	36	VDD	85	DU	86	DU	135	DQ34	136	DQ38	185	VSS	186	VSS
37	/CK0	38	VSS	87	VSS	88	VSS	137	VSS	138	VSS	187	DQ58	188	DQ62
39	VSS	40	VSS	89	CK2	90	VSS	139	DQ35	140	DQ39	189	DQ59	190	DQ63
41	DQ16	42	DQ20	91	/CK2	92	VDD	141	DQ40	142	DQ44	191	VDD	192	VDD
43	DQ17	44	DQ21	93	VDD	94	VDD	143	VDD	144	VDD	193	SDA	194	SA0
45	VDD	46	VDD	95	CKE1	96	CKE0	145	DQ41	146	DQ45	195	SCL	196	SA1
47	DQS2	48	DM2	97	DU	98	DU	147	DQS5	148	DM5	197	VDDSPD	198	SA2
49	DQ18	50	DQ22	99	A12	100	A11	149	VSS	150	VSS	199	VDDID	200	NC,TEST

note:
1. Pins 71, 72, 73, 74,77,78,79, 80, 83, 84 are reserved for x72 variants of this module and are not used on the x64 versions.
2. Pin 86 is reserved for a registered variant of this module and is not used on the unbuffered version.
3. Pin 89, 91 are reserved for x72 modules or registered modules and is not used on the unbuffered version.
4. Pin 95, 122 are not used for single rank module.
5. Pin 123 is "NC" for 256MB, 512MB, and 1GB, or "A13" for 2GB module.

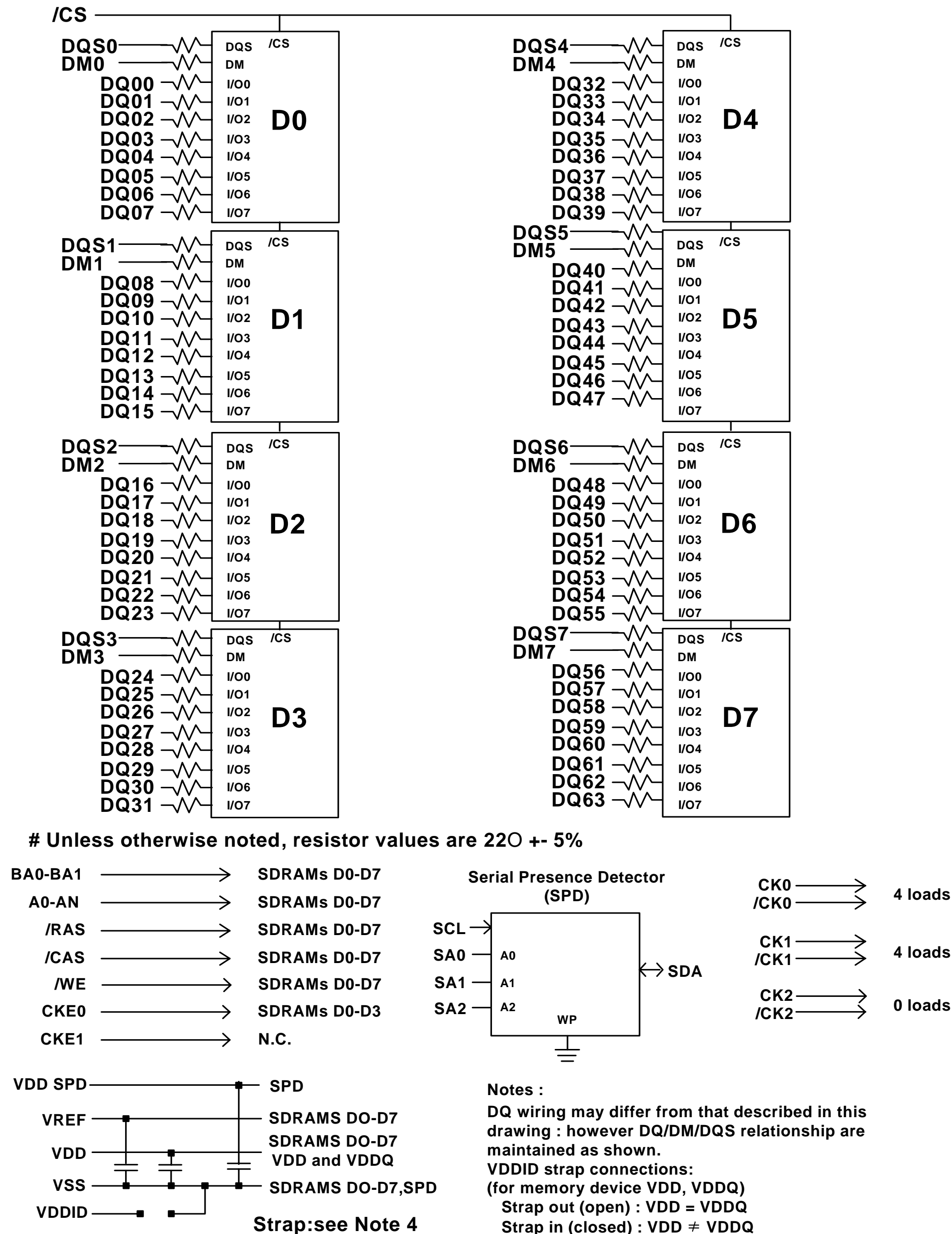
FUNCTIONAL BLOCK DIAGRAM

128MB, 16M x 64 Unbuffered SO-DIMM: HYMD216M646D[L][P]6

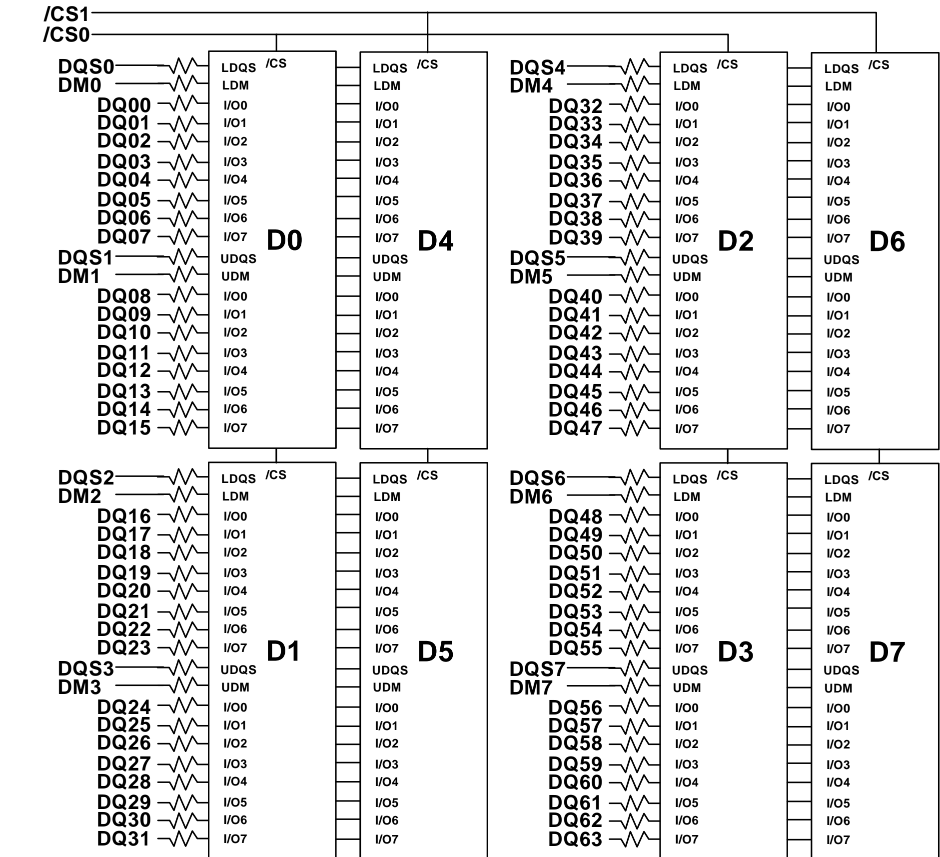


FUNCTIONAL BLOCK DIAGRAM

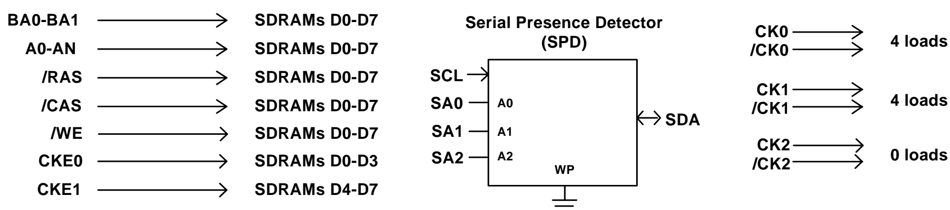
256MB, 32M x 64 Unbuffered SO-DIMM: HYMD232M646D[L][P]8

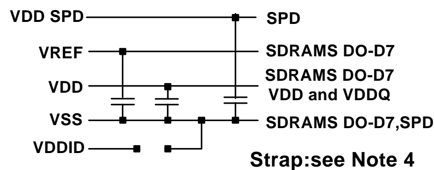


FUNCTIONAL BLOCK DIAGRAM
256MB, 32M x 64 Unbuffered SO-DIMM: HYMD232M646D[L][P]6



Unless otherwise noted, resistor values are 22Ω +- 5%





Strap:see Note 4

Notes :
DQ wiring may differ from that described in this drawing : however DQ/DM/DQS relationship are maintained as shown.
VDDID strap connections:
(for memory device VDD, VDDQ)
Strap out (open) : VDD = VDDQ
Strap in (closed) : VDD ≠ VDDQ

ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Symbol	Rating	Unit
Operating Temperature (Ambient)	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 150	°C
Voltage on VDD relative to VSS	VDD	-1.0 ~ 3.6	V
Voltage on VDDQ relative to VSS	VDDQ	-1.0 ~ 3.6	V
Voltage on inputs relative to Vss	VINPUT	-1.0 ~ 3.6	V
Voltage on I/O pins relative to Vss	VIO	-0.5 ~3.6	V
Output Short Circuit Current	IOS	50	mA
Soldering Temperature · Time	TSOLDER	260 · 10	°C · Sec

Note:
1. Operation at above absolute maximum rating can adversely affect device reliability

DC OPERATING CONDITIONS (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

Parameter		Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage (DDR 200, 266, 333)		VDD	2.3	2.5	2.7	V	
Power Supply Voltage (DDR 400)		VDD	2.5	2.6	2.7	V	2
Power Supply Voltage (DDR 200, 266, 333)		VDDQ	2.3	2.5	2.7	V	1
Power Supply Voltage (DDR 400)		VDDQ	2.5	2.6	2.7	V	1,2
Input High Voltage		VIH	VREF + 0.15	-	VDDQ + 0.3	V	
Input Low Voltage		VIL	-0.3	-	VREF - 0.15	V	3
Termination Voltage		VTT	VREF - 0.04	VREF	VREF + 0.04	V	
Reference Voltage		VREF	0.49*VDDQ	0.5*VDDQ	0.51*VDDQ	V	4
Input Voltage Level, CK and $\overline{CK}$ inputs		VIN(DC)	-0.3	-	VDDQ+0.3	V	
Input Differential Voltage, CK and CK inputs		VID(DC)	0.36	-	VDDQ+0.6	V	5
V-I Matching: Pullup to Pulldown Current Ratio		VI(RATIO)	0.71	-	1.4	-	6
Input Leakage Current		ILI	-2	-	2	uA	7
Output Leakage Current		ILO	-5	-	5	uA	8
Normal Strength Output Driver (VOUT=VTT ± 0.84)	Output High Current (min VDDQ, min VREF, min VTT)	IOH	-16.8	-	-	mA	
	Output Low Current (min VDDQ, max VREF, max VTT)	IOL	16.8	-	-	mA	
Half Strength Output Driver (VOUT=VTT ± 0.68)	Output High Current (min VDDQ, min VREF, min VTT)	IOH	-13.6	-	-	mA	
	Output Low Current (min VDDQ, max VREF, max VTT)	IOL	13.6	-	-	mA	

Note:
1. VDDQ must not exceed the level of VDD.
2. For DDR400, VDD=2.6V ± 0.1V, VDDQ=2.6V ± 0.1V
3. VIL (min) is acceptable -1.5V AC pulse width with ≤ 5ns of duration.
4. VREF is expected to be equal to 0.5*VDDQ of the transmitting device, and to track variations in the dc level of the same. Peak to peak noise on VREF may not exceed ± 2% of the DC value.
5. VID is the magnitude of the difference between the input level on CK and the input level on /CK.
6. The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages from 0.25V to 1.0V. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1/7 for device drain to source voltages from 0.1 to 1.0.
7. VIN=0 to VDD, All other pins are not tested under VIN =0V.
8. DQs are disabled, VOUT=0 to VDDQ.

IDD SPECIFICATION AND CONDITIONS (TA=0 to 70°C, Voltage referenced to VSS = 0V)

128MB, 32M x 64 Unbuffered SO-DIMM: HYMD216M646D[L][P]6

Symbol	Test Condition	Speed				Unit	Note
		-D43	-J	-K	-H		
IDD0	One bank; Active - Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	360	320	280	280	mA	
IDD1	One bank; Active - Read - Precharge; Burst Length=2; tRC=tRC(min); tCK=tCK(min); address and control inputs changing once per clock cycle	400	400	360	360	mA	
IDD2P	All banks idle; Power down mode; CKE=Low, tCK=tCK(min)	40	40	40	40	mA	
IDD2F	/CS=High, All banks idle; tCK=tCK(min); CKE= High; address and control inputs changing once per clock cycle. VIN=VREF for DQ, DQS and DM	240	200	160	160	mA	
IDD3P	One bank active; Power down mode; CKE=Low, tCK=tCK(min)	60	60	60	60	mA	
IDD3N	/CS=HIGH; CKE=HIGH; One bank; Active-Precharge; tRC=tRAS(max); tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	160	140	120	120	mA	
IDD4R	Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOUT=0mA	800	760	680	680	mA	
IDD4W	Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle	800	760	680	680	mA	
IDD5	tRC=tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR266B at 133Mhz; distributed refresh	600	560	520	520	mA	
IDD6	CKE=<0.2V; External clock on; tCK =tCK(min) — Normal	12	12	12	12	mA	
	Low Power	6	6	6	6	mA	
IDD7	Four bank interleaving with BL=4 Refer to the following page for detailed test condition	1000	960	880	880	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

IDD SPECIFICATION AND CONDITIONS (TA=0 to 70°C, Voltage referenced to VSS = 0V)

256MB, 32M x 64 Unbuffered SO-DIMM: HYMD232M646D[L][P]8

Symbol	Test Condition	Speed				Unit	Note
		-D43	-J	-K	-H		
IDD0	One bank; Active - Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	720	640	560	560	mA	
IDD1	One bank; Active - Read - Precharge; Burst Length=2; tRC=tRC(min); tCK=tCK(min); address and control inputs changing once per clock cycle	800	800	720	720	mA	
IDD2P	All banks idle; Power down mode; CKE=Low, tCK=tCK(min)	80	80	80	80	mA	
IDD2F	/CS=High, All banks idle; tCK=tCK(min); CKE= High; address and control inputs changing once per clock cycle. VIN=VREF for DQ, DQS and DM	480	400	320	320	mA	
IDD3P	One bank active; Power down mode; CKE=Low, tCK=tCK(min)	120	120	120	120	mA	
IDD3N	/CS=HIGH; CKE=HIGH; One bank; Active-Precharge; tRC=tRAS(max); tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	400	360	320	320	mA	
IDD4R	Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOUT=0mA	1440	1280	1200	1200	mA	
IDD4W	Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle	1440	1280	1200	1200	mA	
IDD5	tRC=tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR266B at 133Mhz; distributed refresh	1200	1200	1120	1120	mA	
IDD6	CKE=<0.2V; External clock on; tCK =tCK(min) — Normal	24	24	24	24	mA	
	Low Power	12	12	12	12	mA	
IDD7	Four bank interleaving with BL=4 Refer to the following page for detailed test condition	1840	1760	1600	1600	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

IDD SPECIFICATION AND CONDITIONS (TA=0 to 70°C, Voltage referenced to VSS = 0V)

256MB, 32M x 64 Unbuffered SO-DIMM: HYMD232M646D[L][P]6

Symbol	Test Condition		Speed				Unit	Note
			DDR400B	DDR333	DDR266A	DDR266B		
IDD0	One bank; Active - Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle		600	520	440	440	mA	
IDD1	One bank; Active - Read - Precharge; Burst Length=2; tRC=tRC(min); tCK=tCK(min); address and control inputs changing once per clock cycle		640	600	520	520	mA	
IDD2P	All banks idle; Power down mode; CKE=Low, tCK=tCK(min)		80	80	80	80	mA	
IDD2F	/CS=High, All banks idle; tCK=tCK(min); CKE= High; address and control inputs changing once per clock cycle. VIN=VREF for DQ, DQS and DM		480	400	320	320	mA	
IDD3P	One bank active; Power down mode; CKE=Low, tCK=tCK(min)		120	120	120	120	mA	
IDD3N	/CS=HIGH; CKE=HIGH; One bank; Active-Precharge; tRC=tRAS(max); tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		440	380	320	320	mA	
IDD4R	Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOUT=0mA		1040	960	840	840	mA	
IDD4W	Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle		1040	960	840	840	mA	
IDD5	tRC=tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR266B at 133Mhz; distributed refresh		840	800	720	720	mA	
IDD6	CKE=<0.2V; External clock on; tCK =tCK(min)	Normal	24	24	24	24	mA	
		Low Power	12	12	12	12	mA	
IDD7	Four bank interleaving with BL=4 Refer to the following page for detailed test condition		1240	1160	1040	1040	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

AC OPERATING CONDITIONS (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

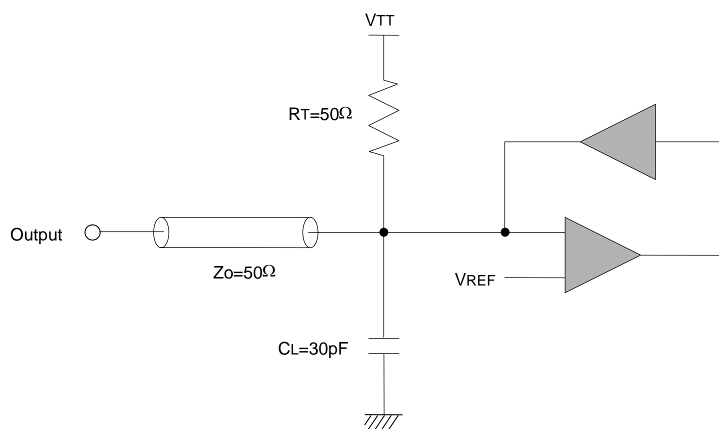
Parameter	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.31	-	V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	VIL(AC)	-	VREF - 0.31	V	
Input Differential Voltage, CK and /CK inputs	VID(AC)	0.7	VDDQ + 0.6	V	1
Input Crossing Point Voltage, CK and /CK inputs	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

Note:
1. VID is the magnitude of the difference between the input level on CK and the input on /CK.
2. The value of VIX is expected to equal 0.5*V DDQ of the transmitting device and must track variations in the DC level of the same.

AC OPERATING TEST CONDITIONS (TA=0 to 70°C, Voltage referenced to VSS = 0V)

Parameter	Value	Unit
Reference Voltage	VDDQ x 0.5	V
Termination Voltage	VDDQ x 0.5	V
AC Input High Level Voltage (VIH, min)	VREF + 0.31	V
AC Input Low Level Voltage (VIL, max)	VREF - 0.31	V
Input Timing Measurement Reference Level Voltage	VREF	V
Output Timing Measurement Reference Level Voltage	VTT	V
Input Signal maximum peak swing	1.5	V
Input minimum Signal Slew Rate	1	V/ns
Termination Resistor (RT)	50	Ω
Series Resistor (RS)	25	Ω
Output Load Capacitance for Access Time Measurement (CL)	30	pF

OUTPUT LOAD CIRCUIT



CAPACITANCE (TA=25°C, f=100MHz)

128MB: HYMD216M646D[L][P]6

Input/Output Pins	Symbol	Min	Max	Unit
A0 ~ A12, BA0, BA1	CIN1	28	40	pF
/RAS, /CAS, /WE	CIN2	28	40	pF
CKE0, CKE1	CIN3	28	40	pF
/CS0, /CS1	CIN4	28	40	pF
CK0, /CK0, CK1, /CK1, CK2, /CK2	CIN5	16	25	pF
DM0 ~ DM7	CIN6	7	12	pF
DQ0 ~ DQ63, DQS0 ~ DQS7	CIO1	7	12	pF

256MB: HYMD232M646D[L][P]8

Input/Output Pins	Symbol	Min	Max	Unit
A0 ~ A12, BA0, BA1	CIN1	36	48	pF
/RAS, /CAS, /WE	CIN2	36	48	pF
CKE0	CIN3	36	40	pF
/CS	CIN4	36	40	pF
CK0, /CK0, CK1, /CK1, CK2, /CK2	CIN5	18	27	pF
DM0 ~ DM7	CIN6	7	12	pF
DQ0 ~ DQ63, DQS0 ~ DQS7	CIO1	7	12	pF

256MB: HYMD232M646D[L][P]6

Input/Output Pins	Symbol	Min	Max	Unit
A0 ~ A12, BA0, BA1	CIN1	36	48	pF
/RAS, /CAS, /WE	CIN2	36	48	pF
CKE0, CKE1	CIN3	28	40	pF
/CS0, /CS1	CIN4	28	40	pF
CK0, /CK0, CK1, /CK1, CK2, /CK2	CIN5	18	27	pF
DM0 ~ DM7	CIN6	12	18	pF
DQ0 ~ DQ63, DQS0 ~ DQS7	CIO1	12	18	pF

AC CHARACTERISTICS (note: 1 - 9 / AC operating conditions unless otherwise noted)

Parameter	Symbol	DDR400B		DDR333		DDR266A		DDR266B		DDR200		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Row Cycle Time	tRC	55	-	60	-	65	-	65	-	70	-	ns
Auto Refresh Row Cycle Time	tRFC	70	-	72	-	75	-	75	-	80	-	ns
Row Active Time	tRAS	40	70K	42	70K	45	120K	45	120K	50	120K	ns
Active to Read with Auto Precharge Delay	tRAP	tRCD or tRASmin	-	tRCD or tRASmin	-	tRCD or tRASmin	-	tRCD or tRASmin	-	tRCD or tRASmin	-	ns
Row Address to Column Address Delay	tRCD	15	-	18	-	20	-	20	-	20	-	ns
Row Active to Row Active Delay	tRRD	10	-	12	-	15	-	15	-	15	-	ns
Column Address to Column Address Delay	tCCD	1	-	1	-	1	-	1	-	1	-	tCK
Row Precharge Time	tRP	15	-	18	-	20	-	20	-	20	-	ns
Write Recovery Time	tWR	15	-	15	-	15	-	15	-	15	-	ns
Internal Write to Read Command Delay	tWTR	2	-	1	-	1	-	1	-	1	-	tCK
Auto Precharge Write Recovery + Precharge Time[22]	tDAL	(tWR/ tCK) + (tRP/tCK)	-	(tWR/ tCK) + (tRP/tCK)	-	(tWR/ tCK) + (tRP/tCK)	-	(tWR/ tCK) + (tRP/tCK)	-	(tWR/ tCK) + (tRP/tCK)	-	tCK
System Clock Cycle Time[24] CL = 3	tCK	5	10	-	-	-	-	-	-	-	-	
System Clock Cycle Time[24] CL = 2.5	tCK	-	-	6	12	7.5	12	7.5	12	8.0	12	ns
System Clock Cycle Time[24] CL = 2	tCK	-	-	7.5	12	7.5	12	10	12	10	12	ns
Clock High Level Width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK
Clock Low Level Width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK
Data-Out edge to Clock edge Skew	tAC	-0.7	0.7	-0.7	0.7	-0.75	0.75	-0.75	0.75	-0.75	0.75	ns
DQS-Out edge to Clock edge Skew	tDQSCK	-0.55	0.55	-0.6	0.6	-0.75	0.75	-0.75	0.75	-0.75	0.75	ns
DQS-Out edge to Data-Out edge Skew[21]	tDQSQ	-	0.4	-	0.45	-	0.5	-	0.5	-	0.6	ns
Data-Out hold time from DQS[20]	tQH	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	ns
Clock Half Period[19,20]	tHP	min (tCL,tCH)	-	min (tCL,tCH)	-	min (tCL,tCH)	-	min (tCL,tCH)	-	min (tCL,tCH)	-	ns
Data Hold Skew Factor[20]	tQHS	-	0.5	-	0.55	-	0.75	-	0.75	-	0.75	ns
Valid Data Output Window	tDV	tQH-tDQSQ		tQH-tDQSQ		tQH-tDQSQ		tQH-tDQSQ		tQH-tDQSQ		ns

- Continue

Parameter	Symbol	DDR400B		DDR333		DDR266A		DDR266B		DDR200		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Data-out high-impedance window from CK,/CK[10]	tHZ	-0.7	0.7	-0.7	0.7	-0.75	0.75	-0.75	0.75	-0.8	0.8	ns
Data-out low-impedance window from CK, /CK[10]	tLZ	-0.7	0.7	-0.7	0.7	-0.75	0.75	-0.75	0.75	-0.8	0.8	ns
Input Setup Time (fast slew rate)[14,16-18]	tIS	0.6	-	0.75	-	0.9	-	0.9	-	1.1	-	ns
Input Hold Time (fast slew rate)[14,16-18]	tIH	0.6	-	0.75	-	0.9	-	0.9	-	1.1	-	ns
Input Setup Time (slow slew rate)[15-18]	tIS	0.7	-	0.8	-	1.0	-	1.0	-	1.1	-	ns
Input Hold Time (slow slew rate)[15-18]	tIH	0.7	-	0.8	-	1.0	-	1.0	-	1.1	-	ns
Input Pulse Width[17]	tIPW	2.2	-	2.2	-	2.2	-	2.2	-	2.5	-	ns
Write DQS High Level Width	tDQSH	0.35	-	0.35	-	0.35	-	0.35	-	0.35	-	tCK
Write DQS Low Level Width	tDQSL	0.35	-	0.35	-	0.35	-	0.35	-	0.35	-	tCK
Clock to First Rising edge of DQS-In	tDQSS	0.72	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	tCK
DQS falling edge to CK setup time	tDSS	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	tCK
DQS falling edge hold time from CK	tDSH	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	tCK
DQ & DM input setup time[25]	tDS	0.4	-	0.45	-	0.5	-	0.5	-	0.6	-	ns
DQ & DM input hold time[25]	tDH	0.4	-	0.45	-	0.5	-	0.5	-	0.6	-	ns
DQ & DM Input Pulse Width[17]	tDIPW	1.75	-	1.75	-	1.75	-	1.75	-	2	-	ns
Read DQS Preamble Time	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK
Read DQS Postamble Time	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK
Write DQS Preamble Setup Time[12]	tWPRES	0	-	0	-	0	-	0	-	0	-	ns
Write DQS Preamble Hold Time	tWPREH	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	tCK
Write DQS Postamble Time[11]	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK
Mode Register Set Delay	tMRD	2	-	2	-	2	-	2	-	2	-	tCK
Exit Self Refresh to non-Read command[23]	tXSNR	75	-	75	-	75	-	75	-	80	-	ns
Exit Self Refresh to Read command	tXSRD	200	-	200	-	200	-	200	-	200	-	tCK
Average Periodic Refresh Interval[13,25]	tREFI	-	7.8	-	7.8	-	7.8	-	7.8	-	7.8	us

Note:

1. All voltages referenced to Vss.
2. Tests for ac timing, IDD, and electrical, ac and dc characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Below figure represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).

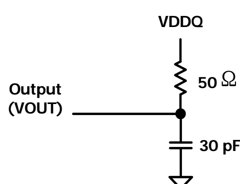


Figure: Timing Reference Load

4. AC timing and IDD tests may use a VIL to VIHswing of up to 1.5 V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK, /CK), and parameter specifications are guaranteed for the specified ac input levels under normal use conditions. The minimum slew rate for the input signals is 1 V/ns in the range between VIL(ac) and VIH(ac).
5. The ac and dc input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the ac input level and will remain in that state as long as the signal does not ring back above (below) the dc input LOW (HIGH) level.
6. Inputs are not recognized as valid until VREF stabilizes. Exception: during the period before VREF stabilizes, CKE $\leq$ 0.2VDDQ is recognized as LOW.
7. The CK, /CK input reference level (for timing referenced to CK, /CK) is the point at which CK and /CK cross; the input reference level for signals other than CK, /CK is VREF.
8. The output timing reference voltage level is VTT.
9. Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
10. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level but specify when the device output is no longer driving (HZ), or begins driving (LZ).
11. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
12. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
13. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
14. For command/address input slew rate $\geq$ 1.0 V/ns.
15. For command/address input slew rate $\geq$ 0.5 V/ns and $<$ 1.0 V/ns
16. For CK & /CK slew rate $\geq$ 1.0 V/ns (single-ended)
17. These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.
18. Slew Rate is measured between VOH(ac) and VOL(ac).
19. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH).
    For example, tCL and tCH are = 50% of the period, less the half period jitter (tJIT(HP)) of the clock source, and less the half period jitter due to crosstalk (tJIT(crosstalk)) into the clock traces.

20.tQH = tHP - tQHS, where:
tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS accounts for 1) The pulse duration distortion of on-chip clock circuits; and 2) The worst case push--out of DQS on one transition followed by the worst case pull--in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.

21. tDQSQ:
Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.

22. tDAL = (tWR/tCK) + (tRP/tCK)
For each of the terms above, if not already an integer, round to the next highest integer.
Example: For DDR266B at CL=2.5 and tCK=7.5 ns
tDAL = ((15 ns / 7.5 ns) + (20 ns / 7.5 ns)) clocks
= ((2) + (3)) clocks
= 5 clocks

23. In all circumstances, tXSNR can be satisfied using
tXSNR = tRFCmin + 1*tCK

24. The only time that the clock frequency is allowed to change is during self-refresh mode.

25. If refresh timing or tDS/tDH is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.

SYSTEM CHARACTERISTICS CONDITIONS for DDR SDRAMS

The following tables are described specification parameters that required in systems using DDR devices to ensure proper performannce. These characteristics are for system simulation purposes and are guaranteed by design.

Input Slew Rate for DQ/DM/DQS (Table a.)

AC CHARACTERISTICS		DDR400		DDR333		DDR266		DDR200		UNIT	Note
PARAMETER	Symbol	min	max	min	max	min	max	min	max		
DQ/DM/DQS input slew rate measured between VIH(DC), VIL(DC) and VIL(DC), VIH(DC)	DCSLEW	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	V/ns	1,12

Address & Control Input Setup & Hold Time Derating (Table b.)

Input Slew Rate	Delta tIS	Delta tIH	UNIT	Note
0.5 V/ns	0	0	ps	9
0.4 V/ns	+50	0	ps	9
0.3 V/ns	+100	0	ps	9

DQ & DM Input Setup & Hold Time Derating (Table c.)

Input Slew Rate	Delta tDS	Delta tDH	UNIT	Note
0.5 V/ns	0	0	ps	11
0.4 V/ns	+75	0	ps	11
0.3 V/ns	+150	0	ps	11

DQ & DM Input Setup & Hold Time Derating for Rise/Fall Delta Slew Rate (Table d.)

Input Slew Rate	Delta tDS	Delta tDH	UNIT	Note
± 0.0 ns/V	0	0	ps	10
± 0.25 ns/V	+50	+50	ps	10
± 0.5 ns/V	+100	+100	ps	10

Output Slew Rate Characteristics (for x4, x8 Devices) (Table e.)

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	Note
Pullup Slew Rate	1.2 - 2.5	1.0	4.5	1,3,4,6,7,8
Pulldown Slew Rate	1.2 - 2.5	1.0	4.5	2,3,4,6,7,8

Output Slew Rate Characteristics (for x16 Device) (Table f.)

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	Note
Pullup Slew Rate	1.2 - 2.5	1.0	4.5	1,3,4,6,7,8
Pulldown Slew Rate	1.2 - 2.5	1.0	4.5	2,3,4,6,7,8

Output Slew Rate Matching Ratio Characteristics (Table g.)

Slew Rate Characteristic	DDR266A		DDR266B		DDR200		Note
Parameter	min	max	min	max	min	max	
Output Slew Rate Matching Ratio (Pullup to Pulldown)	-	-	-	-	0.71	1.4	5,12

Note:

1. Pullup slew rate is characterized under the test conditions as shown in below Figure.

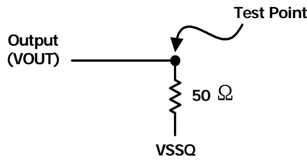


Figure: Pullup Slew rate

2. Pulldown slew rate is measured under the test conditions shown in below Figure.

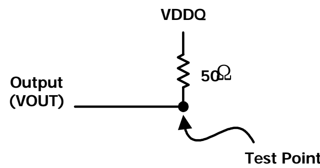


Figure: Pulldown Slew rate

3. Pullup slew rate is measured between (VDDQ/2 - 320 mV ± 250mV)
   Pulldown slew rate is measured between (VDDQ/2 + 320mV ± 250mV)
   Pullup and Pulldown slew rate conditions are to be met for any pattern of data, including all outputs switching and only one output switching.

Example: For typical slew, DQ0 is switching
For minimum slew rate, all DQ bits are switching worst case pattern
For maximum slew rate, only one DQ is switching from either high to low, or low to high.
The remaining DQ bits remain the same as for previous state.

4. Evaluation conditions
   Typical: 25 ^{o}C (Ambient), VDDQ = nominal, typical process
   Minimum: 70 ^{o}C (Ambient), VDDQ = minimum, slow-slow process
   Maximum: 0 ^{o}C (Ambient), VDDQ = Maximum, fast-fast process
5. The ratio of pullup slew rate to pulldown slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.
6. Verified under typical conditions for qualification purposes.
7. TSOP-II package devices only.
8. Only intended for operation up to 256 Mbps per pin.
9. A derating factor will be used to increase tIS and tIH in the case where the input slew rate is below 0.5 V/ns as shown in Table b. The Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions.
10. A derating factor will be used to increase tDS and tDH in the case where DQ, DM, and DQS slew rates differ, as shown in Tables c & d. Input slew rate is based on the larger of AC-AC delta rise, fall rate and DC-DC delta rise, fall rate. Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions. The delta rise/fall rate is calculated as:
    {1/(Slew Rate1)} - {1/(slew Rate2)}
    For example:
    If Slew Rate 1 is 0.5 V/ns and Slew Rate 2 is 0.4 V/ns, then the delta rise, fall rate is -0.5 ns/V. Using the table given, this would result in the need for an increase in tDS and tDH of 100ps.
11. Table c is used to increase tDS and tDH in the case where the I/O slew rate is below 0.5 V/ns. The I/O slew rate is based on the lesser of the AC-AC slew rate and the DC-DC slew rate. The input slew rate is based on the lesser of the slew rates determined by either VIH(ac) to VIL(AC) or VIH(DC) to VIL(DC), and similarly for rising transitions.
12. DQS, DM, and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.

SIMPLIFIED COMMAND TRUTH TABLE

Command		CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	ADDR	A10/AP	BA	Note
Extended Mode Register Set		H	X	L	L	L	L	OP code			1,2
Mode Register Set		H	X	L	L	L	L	OP code			1,2
Device Deselect		H	X	H	X	X	X	X			1
No Operation				L	H	H	H				
Bank Active		H	X	L	L	H	H	RA		V	1
Read		H	X	L	H	L	H	CA	L	V	1
Read with Autoprecharge									H		1,3
Write		H	X	L	H	L	L	CA	L	V	1
Write with Autoprecharge									H		1,4
Precharge All Banks		H	X	L	L	H	L	X	H	X	1,5
Precharge selected Bank									L	V	1
Read Burst Stop		H	X	L	H	H	L	X			1
Auto Refresh		H	H	L	L	L	H	X			1
Self Refresh	Entry	H	L	L	L	L	H	X			1
	Exit	L	H	H	X	X	X				1
				L	H	H	H				
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X			1
				L	H	H	H				1
	Exit	L	H	H	X	X	X				1
				L	H	H	H				1
Active Power Down Mode	Entry	H	L	H	X	X	X	X			1
				L	V	V	V				1
	Exit	L	H	X							1

(H=Logic High Level, L=Logic Low Level, X=Don't Care, V=Valid Data Input, OP Code=Operand Code, NOP=No Operation)

Note:

1. DM states are Don't Care. Refer to below Write Mask Truth Table.
2. OP Code(Operand Code) consists of A0~A12 and BA0~BA1 used for Mode Registering during Extended MRS or MRS. Before entering Mode Register Set mode, all banks must be in a precharge state and MRS command can be issued after tRP period from Precharge command.
3. If a Read with Autoprecharge command is detected by memory component in CK(n), then there will be no command presented to activated bank until CK(n+BL/2+tRP).
4. If a Write with Autoprecharge command is detected by memory component in CK(n), then there will be no command presented to activated bank until CK(n+BL/2+1+tWR+tRP). Write Recovery Time(tWR) is needed to guarantee that the last data has been completely written.
5. If A10/AP is High when Row Precharge command being issued, BA0/BA1 are ignored and all banks are selected to be precharged.

WRITE MASK TRUTH TABLE

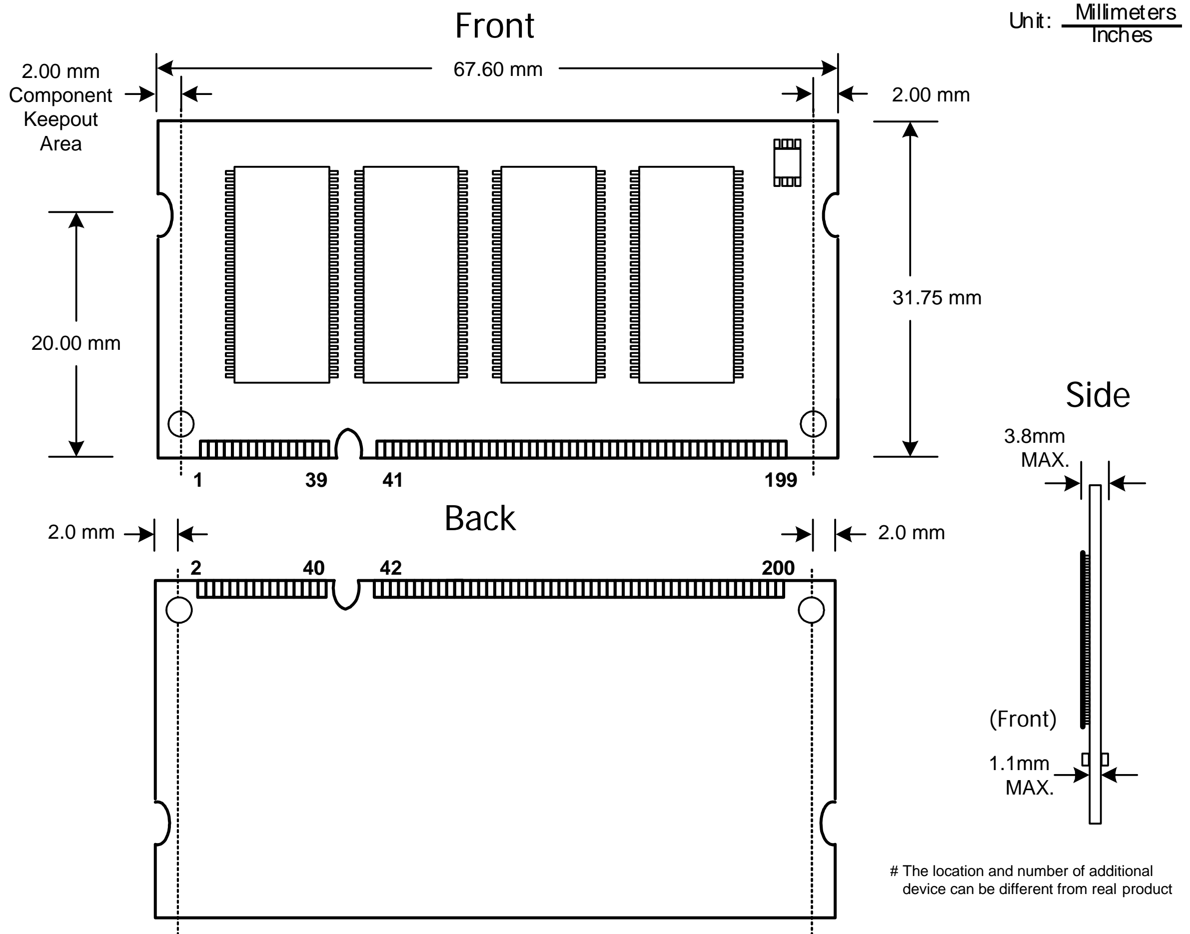
Function	CKEn-1	CKEn	/CS, /RAS, /CAS, /WE	DM	ADDR	A10/AP	BA	Note
Data Write	H	X	X	L	X			1
Data-In Mask	H	X	X	H	X			1

Note:

1. Write Mask command masks burst write data with reference to LDQS/UDQS(Data Strobes) and it is not related with read data. In case of x16 data I/O, LDM and UDM control lower byte(DQ0~7) and Upper byte(DQ8~15) respectively.

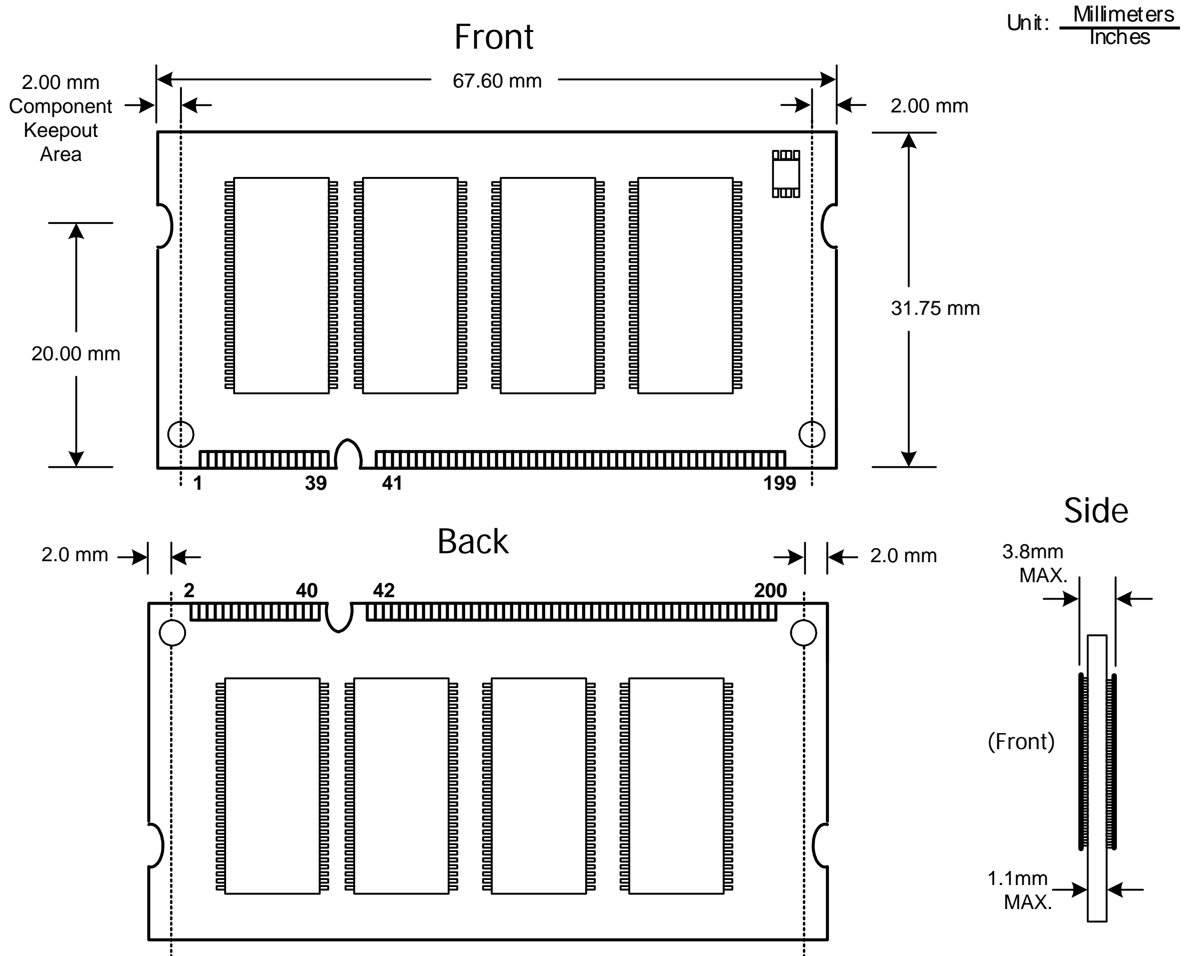
PACKAGE DIMENSIONS

128MB, 16M x 64 Unbuffered SO-DIMM : HYMD216M646D[L][P]6

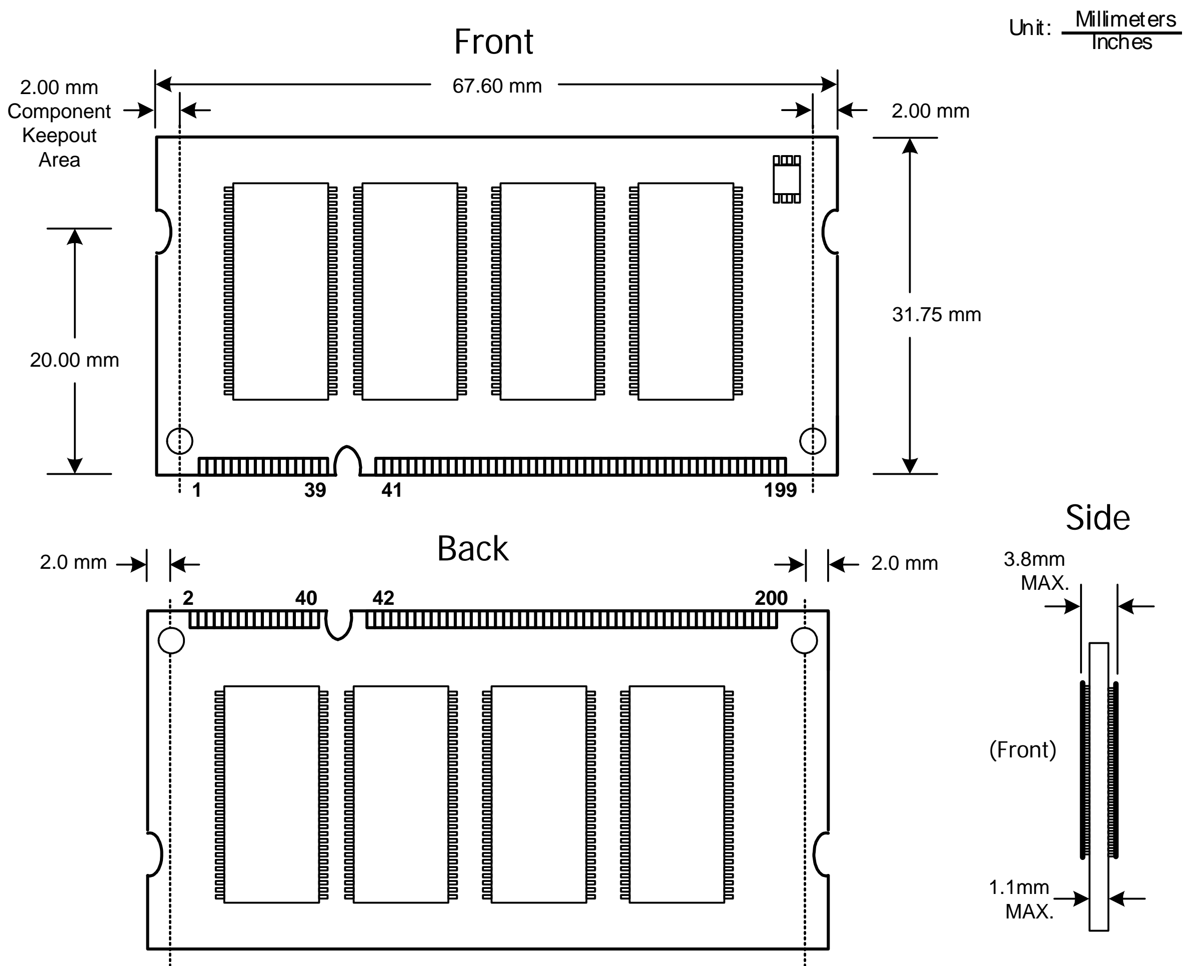


PACKAGE DIMENSIONS

256MB, 32M x 64 Unbuffered SO-DIMM: HYMD232M646D[L][P]8



PACKAGE DIMENSIONS
256MB, 32M x 64 Unbuffered SO-DIMM: HYMD232M646D[L][P]6



REVISION HISTORY

Revision	History	Date	Remark
1.0	First Version Release - Datasheet coverage is changed from an individual module part to a component based module family	Feb. 2005	
1.1	Corrected PIN DESCRIPTION and PIN ASSIGNMENT Tables	May. 2005	